

Software Radio Research for Reconfigurable Wireless Physical Layers

Jeudi 7 octobre 2004

Supélec - Rennes

Christophe Moy
Mitsubishi Electric ITE
Telecommunication Laboratory



outline

- software radio in ITE
- hardware platforms for experiments
- digital radio on generic hardware
- reconfiguration
- design methodology perspectives
- collaborations
- conclusions



software radio research in ITE

- **SWR research in ITE since early 1999**
- **research activity**
- **3 engineers + 1 PhD student**
- **~15 papers in international conference**
- **invitation to IEEE RAWCON'03 SDR Workshop in Boston (Aug. 2003)**
invitation to ANWIRE'2003 in Mykonos, Greece (Oct. 2003)
- **representation of Mitsubishi Electric at SDR Forum & WWRF**
- **Collaborations internally to Mitsubishi Electric**
 - 3 years with Mobile BU in Rennes: MMCE (Trium R&D)
 - 3 years with Semiconductor BU (Renesas now)
- **RNRT A3S - Adéquation Architecture / Application Système**
- **IST E²R - End-to-End Reconfigurability**



what is software radio?

- **digital conversion as close as possible of the antenna**
 - **specialization of the system in the digital domain, if possible in SW**
 - **in order to benefit from the digital domain**
 - design techniques
 - computer aided design tools...
 - technologies
 - low power consumption,
 - small size...
 - digital signal processing advantages for telecommunications
 - robustness, protection capabilities,
 - capacity...
 - reconfigurability
 - processors
 - reconfigurable HW
 - parameterizable ASICs
- real new feature that implies new radio paradigm**



software radio in the large scale

- **many research areas around software radio (examples)**
 - design issues
 - HW components design & technology: processors architecture, FPGA, ADC/DAC, power amplifiers, filters, antennas, MEMS, communication media, SoC, NoC...
 - SW design: compilers, multi-processing, high-level HW/SW co-design & verification, SW frameworks for reconfiguration, distributed management...
 - signal processing
 - digital radio, multi-standard, algorithm parameterization, environment characterization, MIMO...
 - network management
 - inter-standard hand-over, reconfiguration orders management, reconfiguration state management...
 - regulatory aspects
 - type of approval, spectrum management policy, SDR standard...
 - security
 - encryption, protocols...
 - cognitive radio
 - ...



manufacturer's interest in software radio

- **Mitsubishi Electric**
 - 2G infrastructure (PDC, PHS in Japan)
 - 2G mobile phones (PDC & PHS in Japan, GSM/GPRS in Europe and USA)
 - 3G mobile phones (FOMA in Japan)
- **SDR advantages from the infrastructure point of view**
 - system adaptability to specific context
 - system migration from one generation to the other
- **SDR advantages from the mobile manufacturer point of view**
 - time to market - shorter development time
 - same design for several market
 - bug fixing, maintenance
 - multi-mode, multi-standard



areas of interest

- **HW architecture**
 - reconfigurability (potential)
 - processors (SW), reconfigurable HW, parametrizable ASICs
 - computing power (potential)
 - multi-processing (SoC or distributed), heterogeneity
 - communication media
 - **digital radio processing**
 - digital signal processing
 - SW and reconfigurable HW signal processing IPs
 - **SW architecture for reconfiguration**
 - component-based approach
 - OTAR
 - **design methodology for heterogeneous platforms or SoC**
 - concentrating on physical layer
- processing boards and circuits architecture
- IP design methodology
- reconfiguration management
- platform/application abstraction

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requirements for SWR

keywords

- **genericity** (many different applications are possible)
- **heterogeneity** (processors, digital ASICs, analog ASICs, GPP, possible FPGA...)
- **modularity** (many daughter boards are available)
- **scalability** (other boards may be added in the same rack)
- **reconfigurability** (thanks to parametrizable ASICs, processors and FPGAs)
- **portability** (C language whatever processor, VHDL for FPGAs)
- **digital or software IF** (DDC and DUC that are bypassable)
- **ease of use during development stage** (multi-host remote access)
- **SW co-design tools** (automatic code generation)

COTS platforms

all the elements that will be present in future SWR systems

- **heterogeneous computing**
 - programmable (DSP, GPP)
 - reconfigurable HW (FPGA)
 - parameterizable ASIC (DDC, DUC, ADC, DAC)
 - analog ASIC (PA, filters)
- **heterogeneous communications**
 - FIFO, bus, TCP, shared memory
- **digital IF**
 - through parameterizable ASIC (DDC, DUC)
 - directly from DSP or FPGA (bypass ASIC)

processing
mother board



TX: D/A & DUC
daughter board

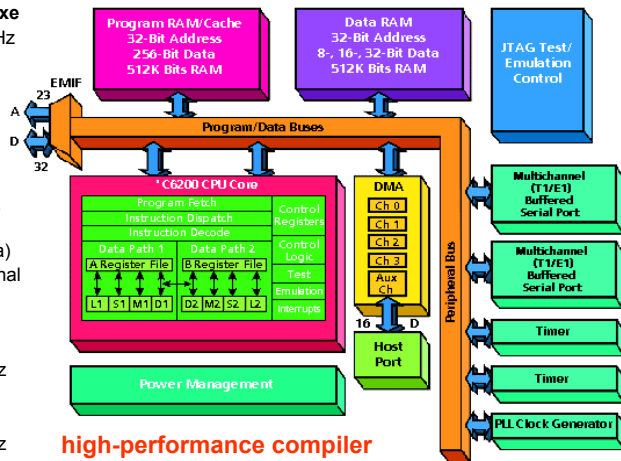


RX: A/D & DDC
daughter board



DSP - C6x processors

- **TMS320C6201 : Virgule fixe**
 - 1600 MIPS @ 200 MHz
- **Architecture VLIW**
 - 8 instructions en parallèle
 - 2 Multiplieurs
 - 6 ALUS
 - software pipeline
- **Mémoire & périphériques**
 - RAM interne 128 kB (64kB prog./64kB data)
 - Interface EMIF (External Memory Interface)
 - 4 Contrôleurs DMA
- **TMS320C6203**
 - 2400 MIPS à 300 MHz
 - RAM: 512 kB /364 kB
- **TMS320C6416**
 - 4800 MIPS à 600 MHz



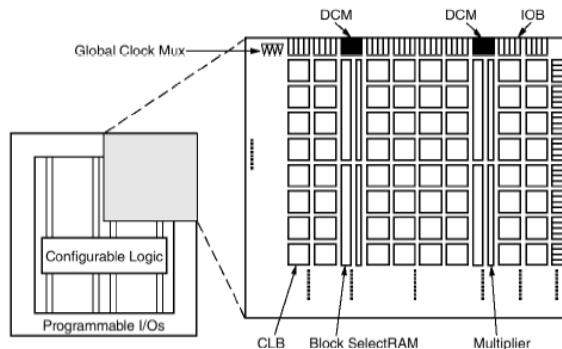
high-performance compiler

ITE research on SDR



FPGA - Virtex-II

- **XC2V3000**
 - 3 million gates
 - 14336 slices
 - 28672 FlipFlops & LUT
 - 1.728 Mbits embedded RAM
 - 448 kbits distributed mem
 - 96 multipliers (18x18 bits)
 - 720 I/O
 - Active interconnect routing matrix
- **XC2V8000**
 - 3.024 Mbits emb. RAM
 - 1456 kbits distributed mem
 - 168 multipliers



ITE research on SDR



generic hardware platforms for experimentation and demos

PENTEK

- **multi-fixed point DSP board**
 - 4 TI C6203 DSPs @300 MHz
 - high speed bi-FIFO comm links
 - host - target ethernet link (100 Mb/s)
- **2 channel wideband Tx module**
 - upconverter (DUC), D/A converter
 - upconverter is bypassable
 - programmable parameters
- **2 channel wideband Rx module**
 - A/D converter, downconverter (DDC)
 - downconverter is bypassable
 - programmable parameters
- **2 x XC2V3000 Xilinx**

LSP LYRtech

- **floating point DSP board**
 - C6701 DSP @166 MHz
- **2 channel wideband Tx/Rx module**
- **XC2V1000 Xilinx**
- **Simulink design to heterogeneous HW direct implementation**

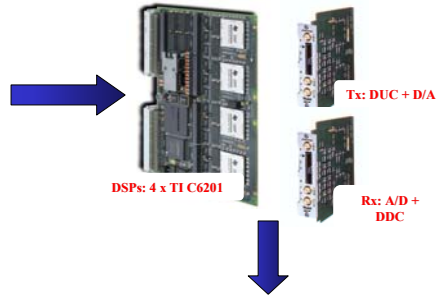
Sundance (DSP+FPGA)

- **in cooperation with IETR/INSA**
 - INSA: Communication Propagation Radar
 - INSA: Image and Teledetection

-
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case study I: timings

	UMTS FDD	GSM/DCS	EDGE	BlueTooth
Symbol rate (kpbs)	3840	270.833	270.833	1000
T (μs)	0.2604 μs	3.69 μs	3.69 μs	1 μs
multiple access	DS-CDMA	FH-TDMA	TDMA	FH-CDMA
time slot	667 μs	576.9 μs	576.9 μs	625 μs 1600 hops/s
modulation	QPSK (DL) BPSK (UL)	GMSK h: 0.5	3π/8 OQset 8-PSK	GFSK h: 0.28 - 0.35
pulse shaping	Root Raised Cosine (RRC) roll off: 0.22	Gaussian (premod) BT: 0.3	Gaussian	Gaussian BT: 0.5
data rate (kbits/s)	144-2000	9.6-13	< 384	1000



Modem	Req. Perf. ksymb/s	Tx Modulator		Rx Demodulator	
		C6201 200MHz	C64x 1GHz	C6201 200MHz	C64x 1GHz
UMTS-HD	3840	960.8	4804	879.1	4395.5
UMTS-FS	3840	1434.2	7172	1435.3	7176.5
GSM	270.83	444.6	2223	753.56	3767.8
EDGE	270.83	1036	5180	506.73	2533.65
Bluetooth	1000	444.6	2223	825.49	4127.45



ITE research on SDR

case study I: timings

	UMTS FDD	GSM
Symbol rate (kpbs)	3840	270
T (μs)	0.2604 μs	3.69 μs

digital processing methods to decrease computational complexity

Modem	Tx Modulator		Rx Demodulator	
	C6201 200MHz	C64x 1GHz	C6201 200MHz	C64x 1GHz
	UMTS-HD	960	4804	879
UMTS-FS	1434	7172	1435	7176.5
GSM	444	2223	753.56	3767.8
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Bluetooth	444	2223	825	4127.45

targeted data rate for R/T

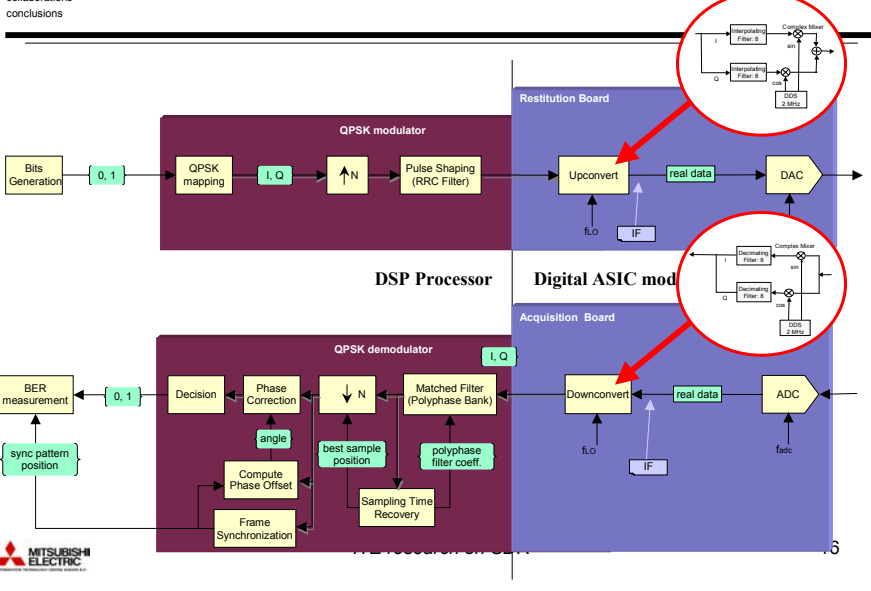
OK @ 200 MHz for GSM & EDGE

ITE research on SDR

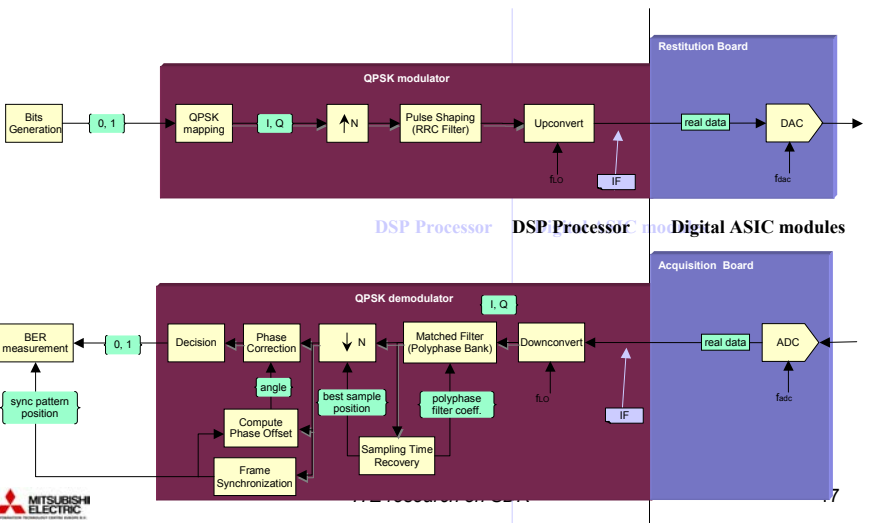
OK @ 1 GHz for all



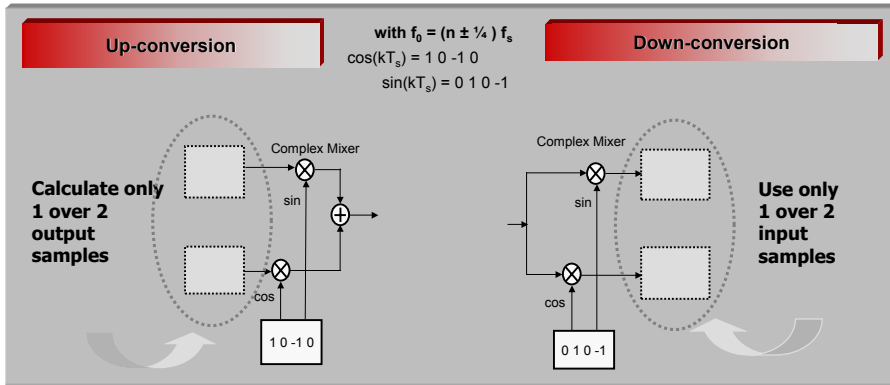
UMTS-HD: mapping on DSPs and ASICs



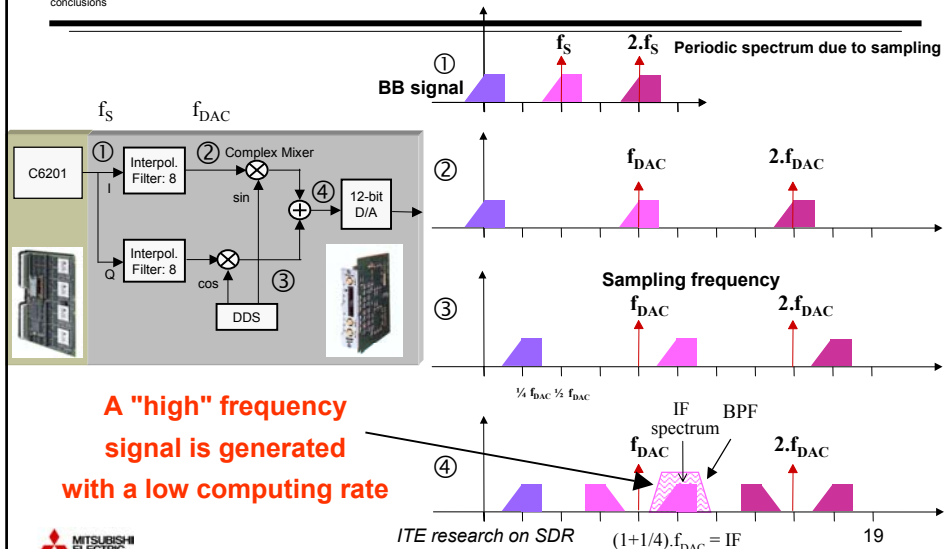
UMTS-FS: full software mapping



fast digital frequency conversion



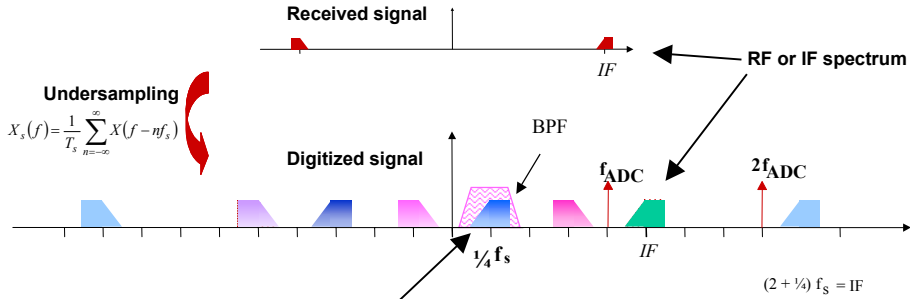
"IF-undersampling" Tx



IF-undersampling Rx

Undersampling

low needs in processing power by reducing sample rate
 $f_s < 2 f_{max}$ $f_s > 2 B$ $f_s = 4 IF/5$



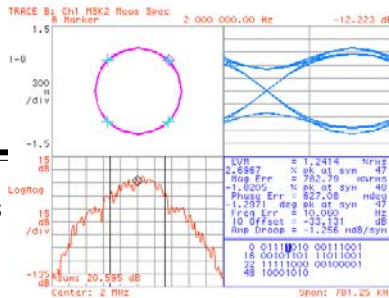
$$X_s(f) = \frac{1}{T_s} (\dots + X(f+3f_s) + X(f+2f_s) + X(f+f_s) + X(f) + X(f-f_s) + X(f-2f_s) + X(f-3f_s) \dots)$$

Signal that will be finally demodulated (low computing rate)

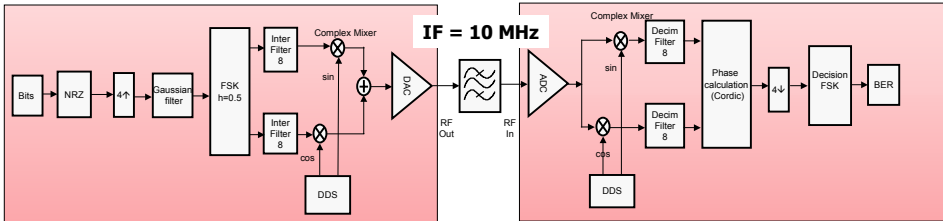


GSM

f_{bits} = 250 kbits/s
 $f_{symbols}$ = 250 ksymbols/s
 over = 4
 $f_{samples}$ = 1 Msamples/s



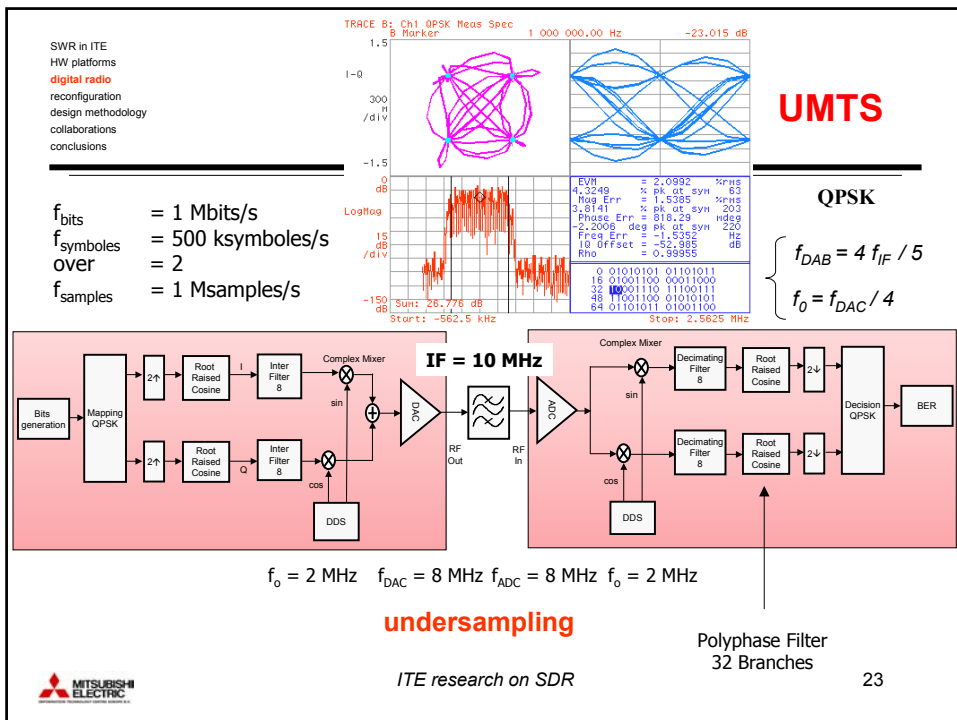
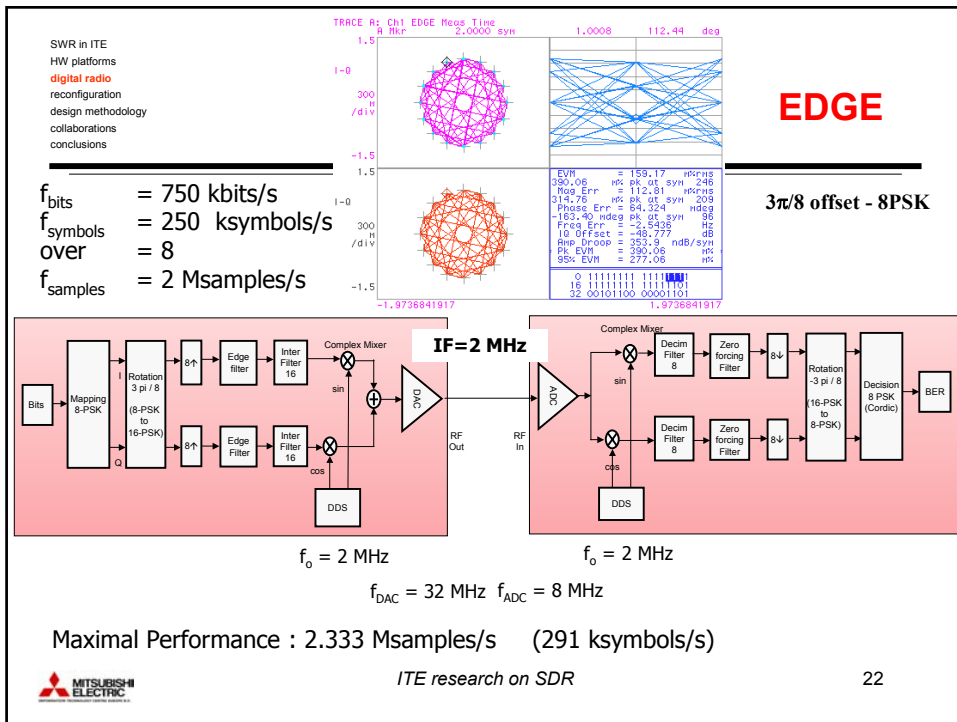
GMSK



Tx Maximal Performance : 1.7 Msamples/s (425 ksymbols/s)

Rx Maximal Performance : 2.7 Msamples/s (675 ksymbols/s)

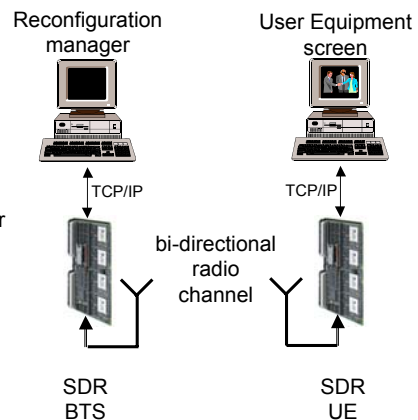




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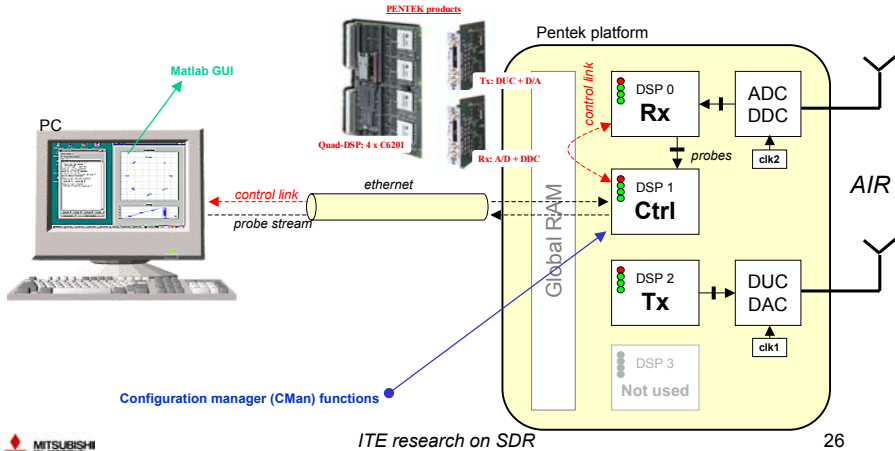
dynamic OTAR by SW download

- real-time video link on a SWR
EDGE standard
- SW patch OTA download
- SDR BTS
 - PC: reconfiguration manager & video server
 - SDR platform
- SDR User Equipment
 - SDR platform supporting real-time reconfiguration without data stream interruption
 - PC for video display

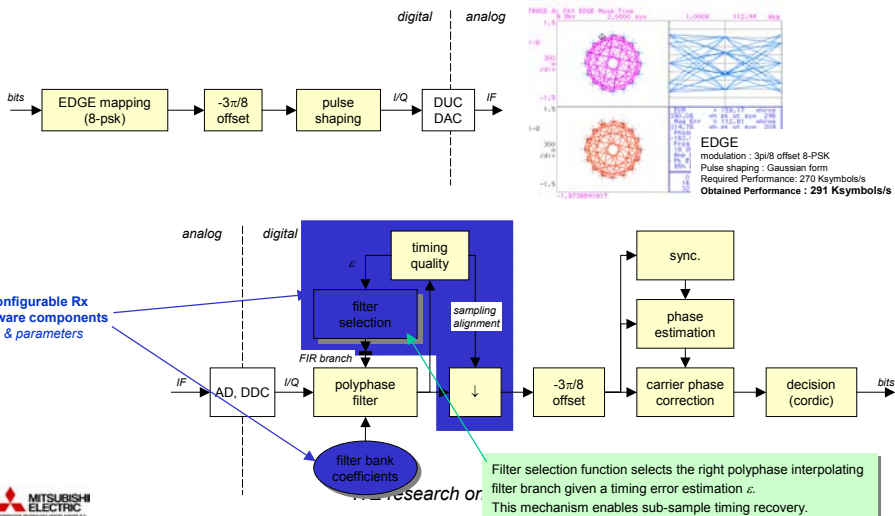


system organization wired reconfiguration

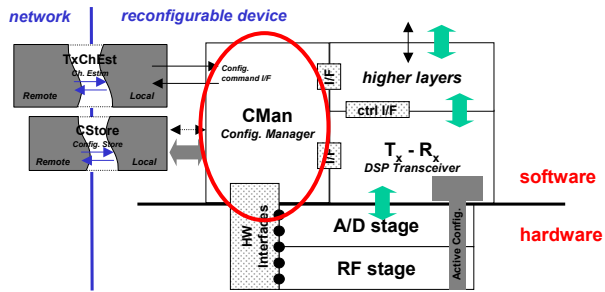
mapping of the application on the hardware



application: EDGE modem (2.75G)



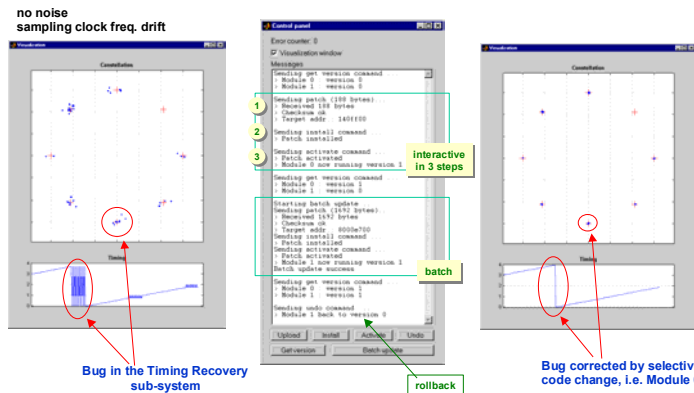
high-level view of the system organization



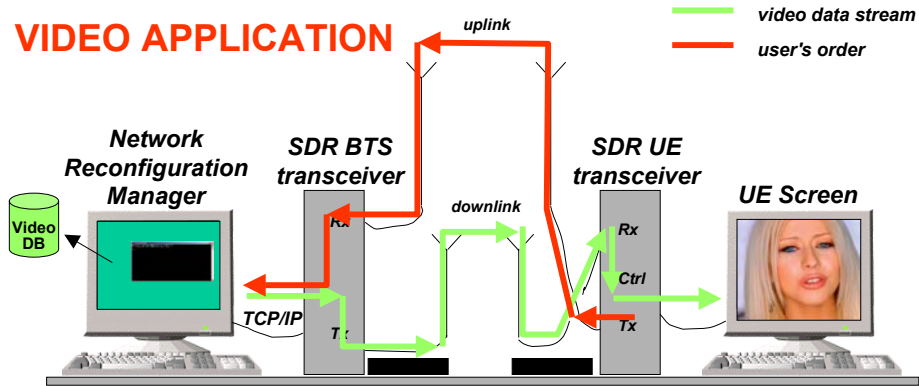
- it can scale to support various operation schemes
 - network independent device reconfiguration
 - network controlled/managed reconfiguration
 - configuration data stored either *locally* or *remotely*
 - decision process under the device responsibility or under network responsibility based on the collection of *relevant measurement data*



network reconfiguration management GUI



VIDEO APPLICATION

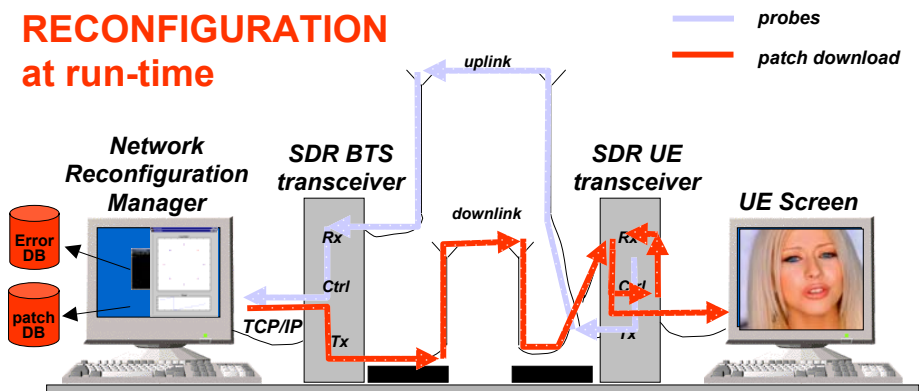


Video service order of the user

- | | |
|--|---|
| 1 - the network has a video database | 5 - EDGE Tx |
| 2 - launch a video server | 6 - EDGE Rx |
| 3 - send the video stream to the BTS | 7 - identification of the service |
| 4 - conversion of the stream to the reconfigurable EDGE protocol stack | 8 - video stream is displayed on the screen |



RECONFIGURATION at run-time

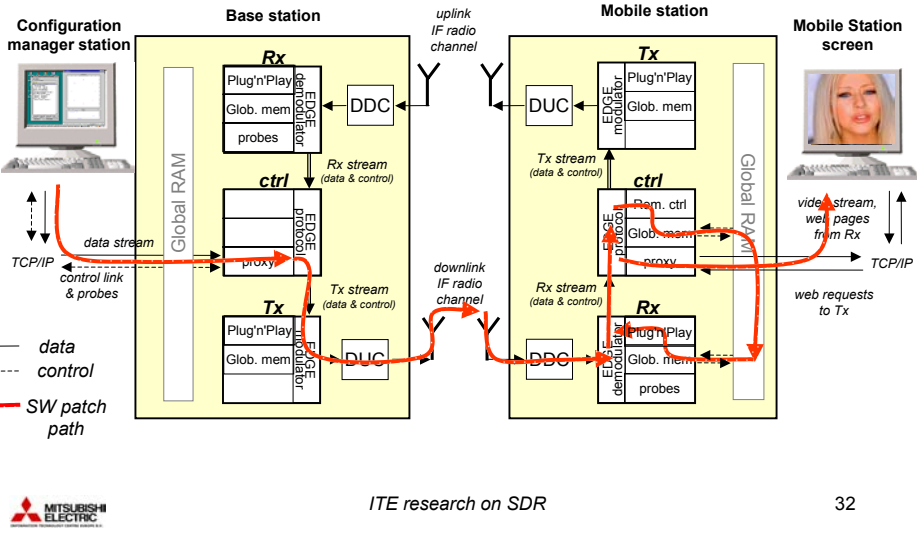


Network reconfiguration manager

- | | |
|---|---|
| 1 - monitors a SDR UE | 5 - download the patch to the UE : circumstances included in the data stream new processing |
| 2 - detects some dysfunction | 6 - separate video from reconfiguration data |
| 3 - identifies the problem | 7 - install reconfiguration data in the UE's Rx internal memory |
| 4 - finds the corresponding patch in its patch database | 8 - activate the patch |
| | 9 - possibly: undo the operation if any problem |



SW download for bug fixing and performance enhancement



business case for real-time reconfiguration

- **manufacturer**
 - bug fixing
 - upgrade capabilities
- **service provider**
 - bug fixing
 - performance enhancement
 - cell capacity optimization (transmit power adaptation)
- **user may benefit in a transparent manner from**
 - battery optimization
 - real-time quality of service management
- **standardization and regulation are needed!**

-
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HW/SW co-design DSP and FPGA

-
- **SWR systems will not only contain processors**
 - today's situation: HW accelerator for highest speed processing
 - medium term: radio applications will be more and more demanding, even if processing power increases
 - **facing co-design is mandatory**
 - **SynDEx for heterogeneous multi-processing**
 - INRIA CAD tool (INRIA: French national research lab in computer sciences)
 - in cooperation with IETR - INSA
 - image processing lab
 - telecom lab
 - Thesis of Mickaël RAULET (3rd year) - memory optimisation

SynDEX for multiprocessing and heterogeneity

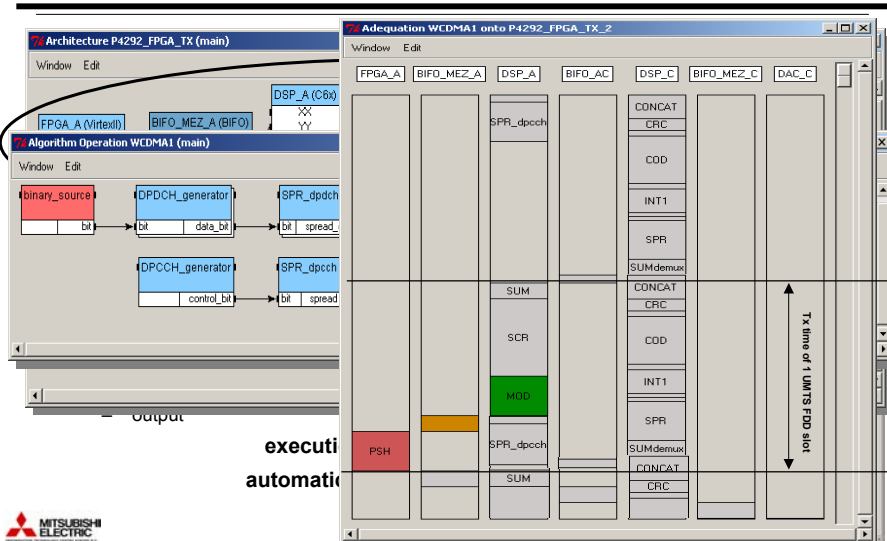
SynDEX entry

- mono-processor version of the code
- description of the algorithm (graph)
- description of the HW architecture (graph)

SynDEX job

- partitioning, scheduling and timing prediction
 - optimized mapping of the algorithms on the HW architecture (heuristic)
 - taking into account both algo execution time and communication delays
- guaranteed functional accuracy with the mono-proc. version
- automatic code generation
- implementation on the target is so fast that verification may be considered in the scope of SynDEX

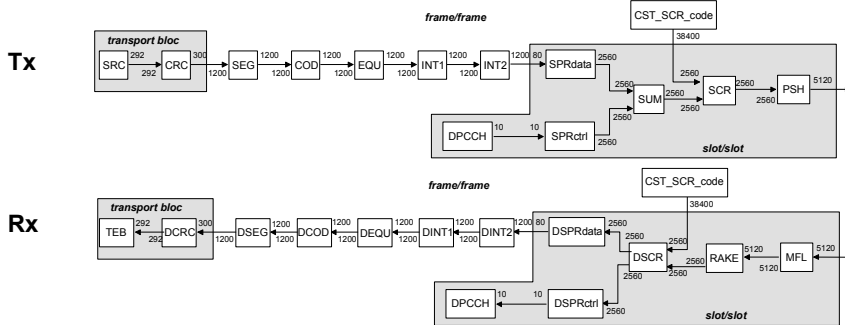
SynDEX



implementations with SynDEX

UMTS FDD uplink modulator / demodulator (Tx: 160 blocs - Rx: 240 blocs)

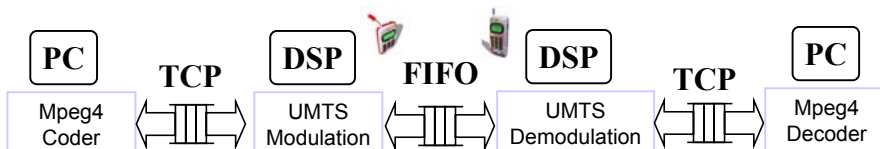
- multi-DSP, FPGA - via FIFO
- multi-GPP - via TCP
- multi-DSP, multi-GPP - via TCP between the platform and the PC



ITE research on SDR

38

MPEG-4 over UMTS



ITE research on SDR

39

In close relationship with Yves SOREL from INRIA Rocquencourt

SynDEX needs to be extended for SWR

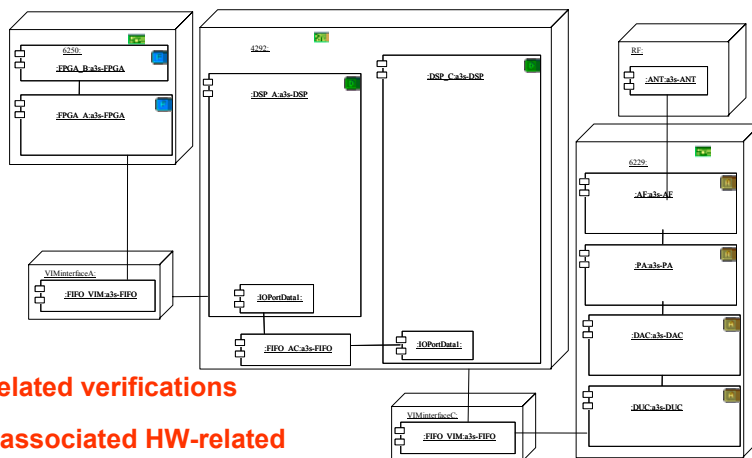
- **only time optimization on both processing and communications**
- **only one processing element by FPGA**

Future work

- **memory: combined optimization with time**
 - data buffer re-organization on each processor (at code generation phase)
 - repartition taking into account time and memory (in the heuristic)
 - thesis of Mickaël RAULET with IETR/INSA
- **FPGA**
 - for parallel multi-processing in the same FPGA (with INSA/IETR)

-
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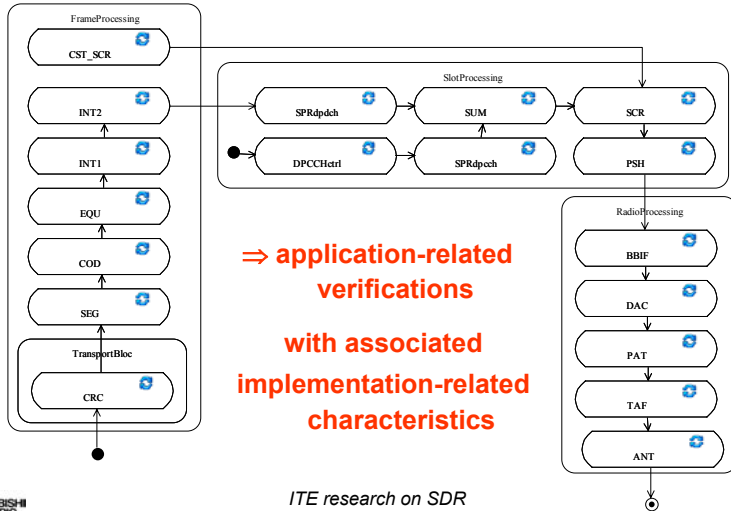
- **Adéquation Architecture / application Système**
 - Thales Comm., Softeam, Lester (Université de Bretagne Sud - Lorient)
 - **Goals**
 - SDR system verification before platform implementation taking into account the SW repartition on the HW
 - **2 UML graphs (UML 1.4) and A3S profile**
 - activity diagram for functional description of the SW application - SW graph
 - deployment diagram for HW platform - HW graph
- first step of verifications (connections...)**
- **generates a XMI file**
 - **verification toolbox**
 - scheduling and execution time
 - memory allocation
 - communication media overload
- either integrated in the UML tool or by web-service**



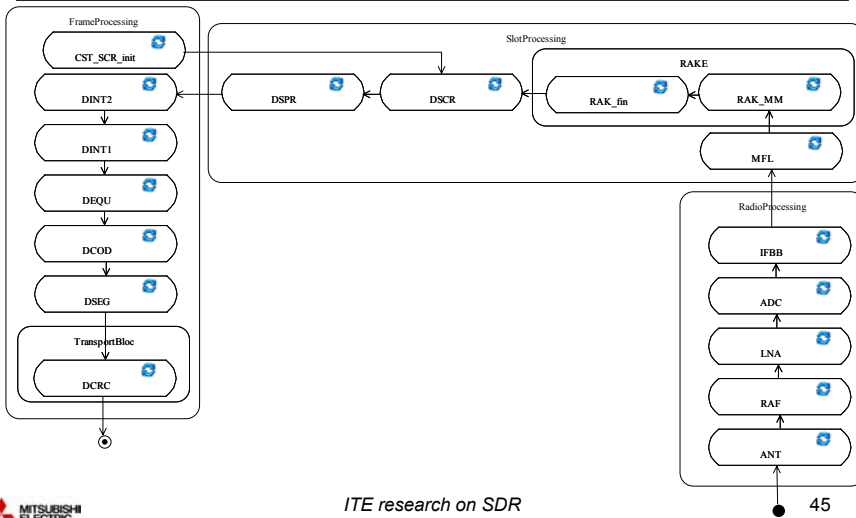
⇒ **HW-related verifications**
with associated HW-related characteristics



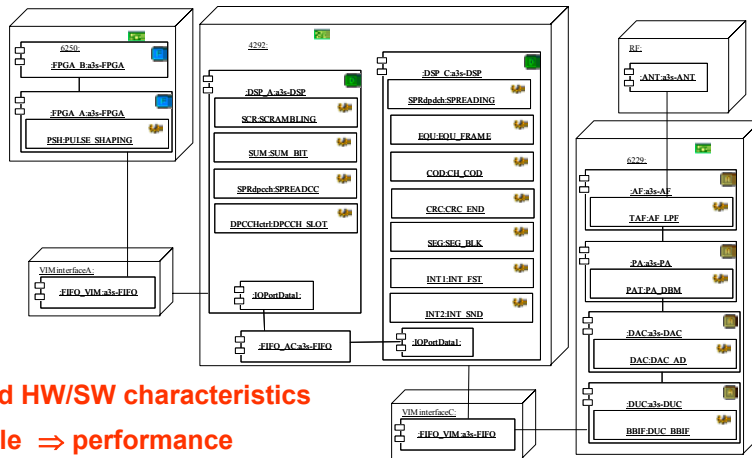
A3S application graph- UMTS Tx



A3S application graph- UMTS Rx



A3S hardware graph - UMTS Tx



combined HW/SW characteristics

⇒ XMI file ⇒ performance

verifications ITE research on SDR



IST E²R

- **End-to-End Reconfigurability**
- **IP project: 28 partners - 8.9 M€**
- **Some of the partners:**
 - Motorola, Siemens, Thales, Nokia, Mitsubishi, Panasonic, Alcatel, NTT DoCoMo, FTR&D, UoAthens, UoSurrey, King's College
- **Work packages**
 - WP1: System Research
 - technical, business and regulatory global approach across all WPs
 - WP2: Equipment Management
 - reconfiguration capabilities of equipments (terminal and BTS)
 - WP3: Network Support for Reconfiguration
 - network management for reconfiguring terminals and network entities
 - WP4: Radio Modem Reconfigurability
 - local configuration control and mechanisms for reliable reconfiguration
 - WP5: Evolution of Radio Resource and Spectrum Management
 - cognitive radio, network-oriented perspectives, spectrum control
 - WP6: E²R Proof of Concept Evolutionary Environment
 - demonstrator
 - WP7: dissemination
 - WP0: administrative



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conclusions

- **software radio research is a very wide research area**
 - necessity to find synergies with partners
 - merge complementary results
- **industrial point of view**
 - implementation is necessary
 - but not always sufficient
- **2G - 2.5G - 3G radio on flexible platforms**
- **SW component-based architecture for Over-the-air SW download**
- **high-level heterogeneous co-design (more and more automatic)**
- **not only for software radio but for other fields: image processing, automotive**