

System on Chip Design Space Exploration: Design Trotter Framework

Jean Philippe Diguët
Guy Gogniat
Jean Luc Philippe

LESTER, UBS - CNRS FRE 2734








SÉMINAIRE SCEE SUPELEC, 21/10/2004


DSE Framework

- Introduction : motivations for DSE
- Target Architecture Model
- System modeling
 - Task Level
 - HCDFG level
- Exploration & Decision Tools :
 - HCDFG-DT : Design Space Exploration & Characterization
 - RT-DT : Exploration, Real Time Scheduling & Partitioning

Introduction : Directions

-  As automotive & avionics before, the issue of SOC design is turning into a question of knowledge management.
 - *"Customization and speed-to-market will drive the industry from the bottom up" [M.J.Bass, HP & M.Christensen, Harvard]*
 - Performances required by users are finally provided => Next challenge : fast design of customized reliable products
 - 75% Reuse & 15% Innovation : 6 months design delay
-  HW/SW On line Debugging and Update
-  CAD Tools for Design Space Exploration & Synthesis
-  RTOS considerations in the HW/SW codesign flow
-  Flexible HW/SW Architectures

Introduction : Directions

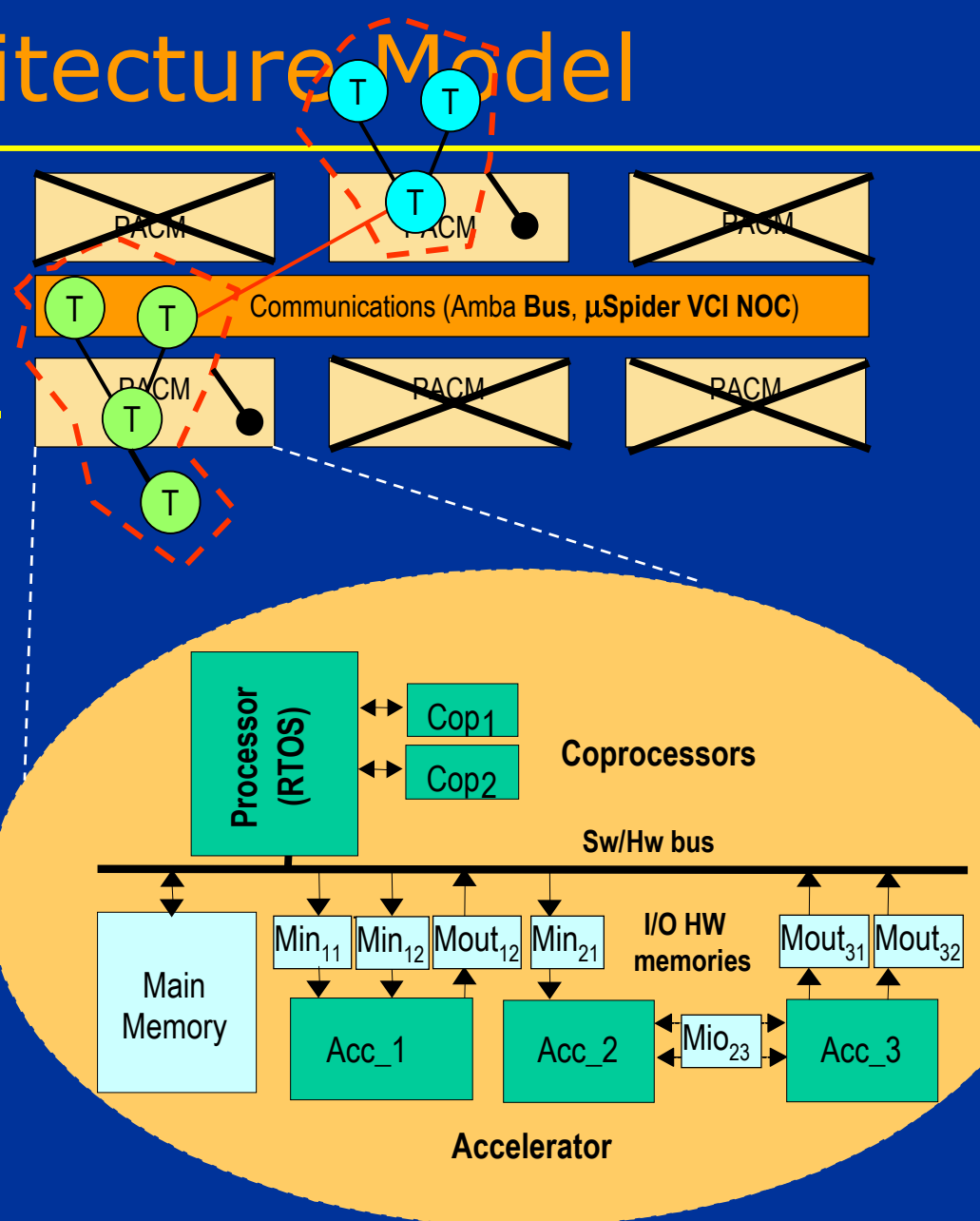
-  (Re)configurable Architectures
 - Improve the Appli/Archi matching: GOPS/Watt & Gops/ μm^2 metrics
 - (Re)configurable architectures:
 - Altera & Xilinx Platform : mixed grain (LUT, DSP blocks) design-time configurable platform (Processor + Memories + DSP blocks + LUT)
 - ARC (ARCTangent), Tensilica (Xtensa), HP/ST (Lx) : Design-time configurable processors => specific instructions => Performances X 10 to 100
 - Academic "Run time" configurable architectures
 - fine grain (LUT), coarse grain (Data Path, ALU, MAC)
 - Industry "run-time" configurable processor : Stretch Inc, PACT,
 - 3G base-station reconfigurable DSP : MorphICs, PicoChip, Morpho Tech.
 - Means (Re) Targetable design flows: HW / SW Ad Hoc Compilers
 - CAD tools for HW/SW exploration & architecture selection before configuration => Design Trotter CAD framework Objectives

Introduction : Objectives

- A System Level Tool Set for Design Space Exploration & Configuration Decision of HW/SW embedded systems
 - Resource Usage & Power optimization => Algo/Archi Matching
 - Research Domain : System Modeling and Design Decision Tools & Methods based on available or coming architectures
- A Pragmatic Approach for real-life constraints
 - Exploration and Design Delay : Key issue => Fast Tools
 - Exploiting usual HW/SW functional block already designed
 - System level estimations cannot be accurate => relative values
 - Static : propose a solution set
 - Dynamic : adaptive configuration

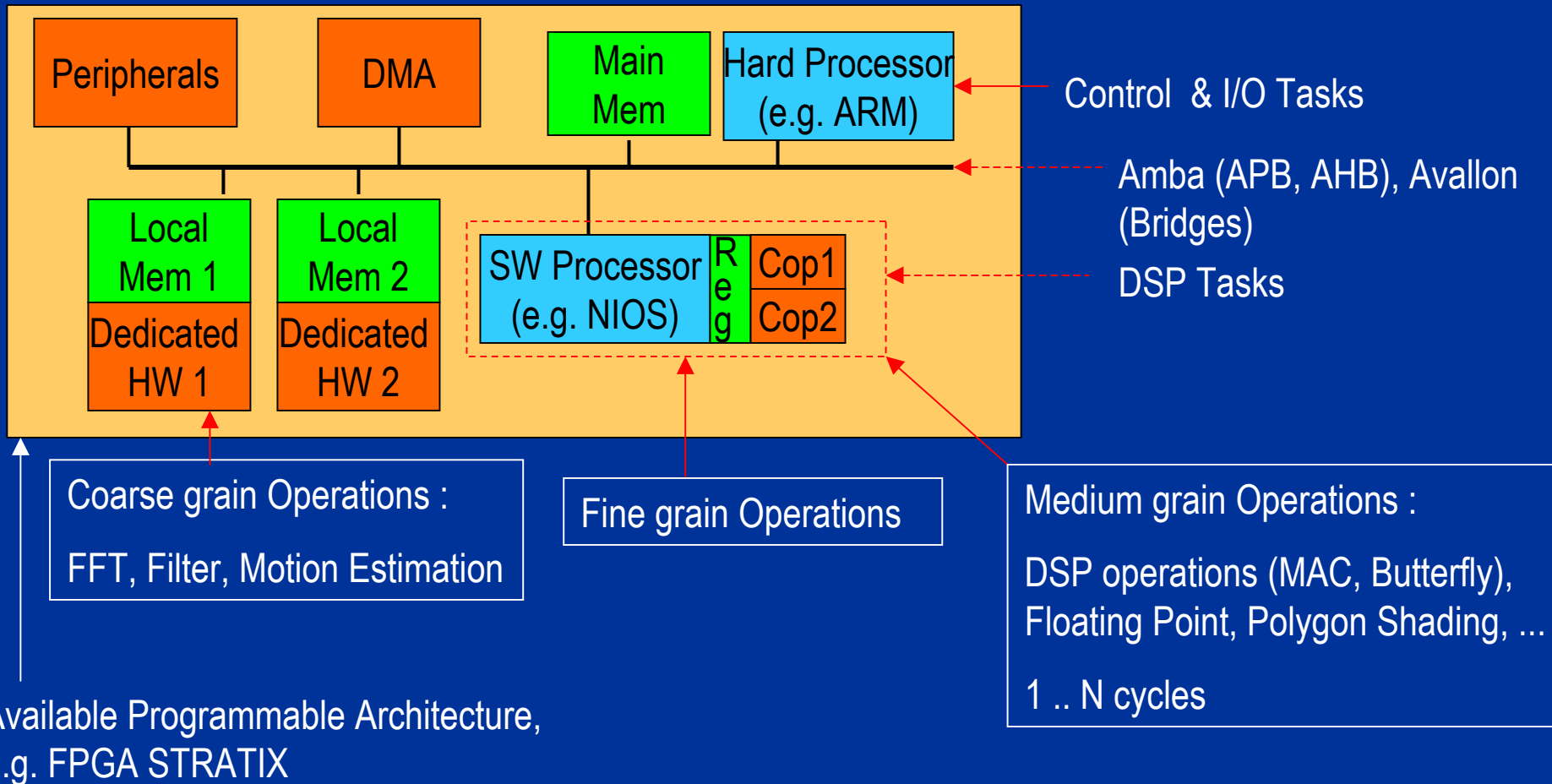
Target Architecture Model

- General Multi-PACM Architecture
- Tasks to PACM assignments with correlation metrics (e.g. Com., Data types, tec.)
- PACM composition :
 - 1 Processor + OS
 - Co-processor acceded through the processor processing registers
 - Accelerators as HW independent modules
- Each PACM designed separately



Target Architecture Model

- An example of a flexible Architecture :



Target Architecture Model

- Architecture parameters
 - generic cost, delay, power computation for various modes

g general features

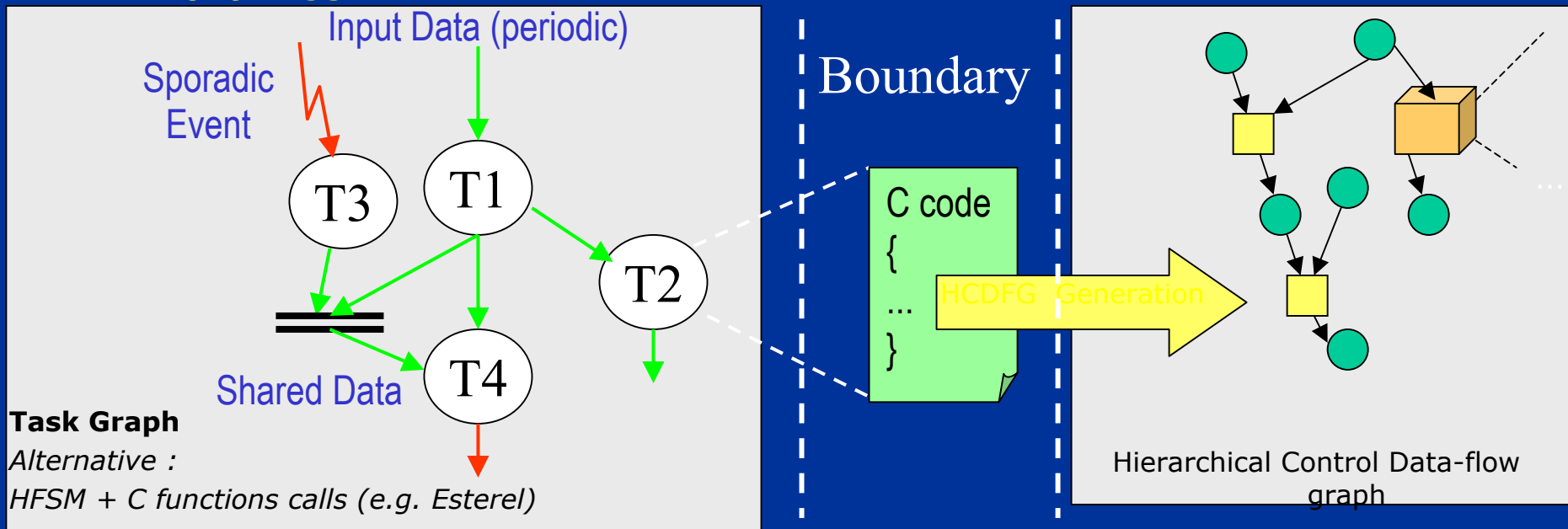
```
{
    AreaUnit      gate
    PwOffUnit     -3 // Power unit (mw)
    TempsUnit     -3 // Time unit

    AreaTaskCom  20 // Communication Task Cost
    MemSwCost    0.01 // Octet cost in SW memory
    MemHwCost    0.02 // Octet cost in HW memory
    SwitchDelay  600 // Context Switching Delay
    PwnSwitch    0.9 // Normalized Power for switching
    AreaCostcom  30
    Pwncom       0.6 // Normalized Power for Communication
}
```

```
c
p Processor
{
    Name      NIOS
    AreaCost  1400
    PwnIdleProc 0.2 // Normalized Idle Power
    BusWidthProc 32
}
b HW/SW Bus
{
    NomBus      AVALLON
    AreaCost    600
    BusWidth    32
    ModeBus     1
    InitDelay   2
    ComDelay    1
}
m Modes 2 // number of modes
m Mode1
{
    ClkPro      300
    ClkHws      200
    ClkBus      100
    VddPro      1.5 // Vdd processor
    VddHws      1.2 // Vdd HW
    PwOffSw     0.02 //SW normalized Static Power/Area
    PwOffHw     0.015 //HW normalized Static Power/Area
}
m Mode2 ...
```

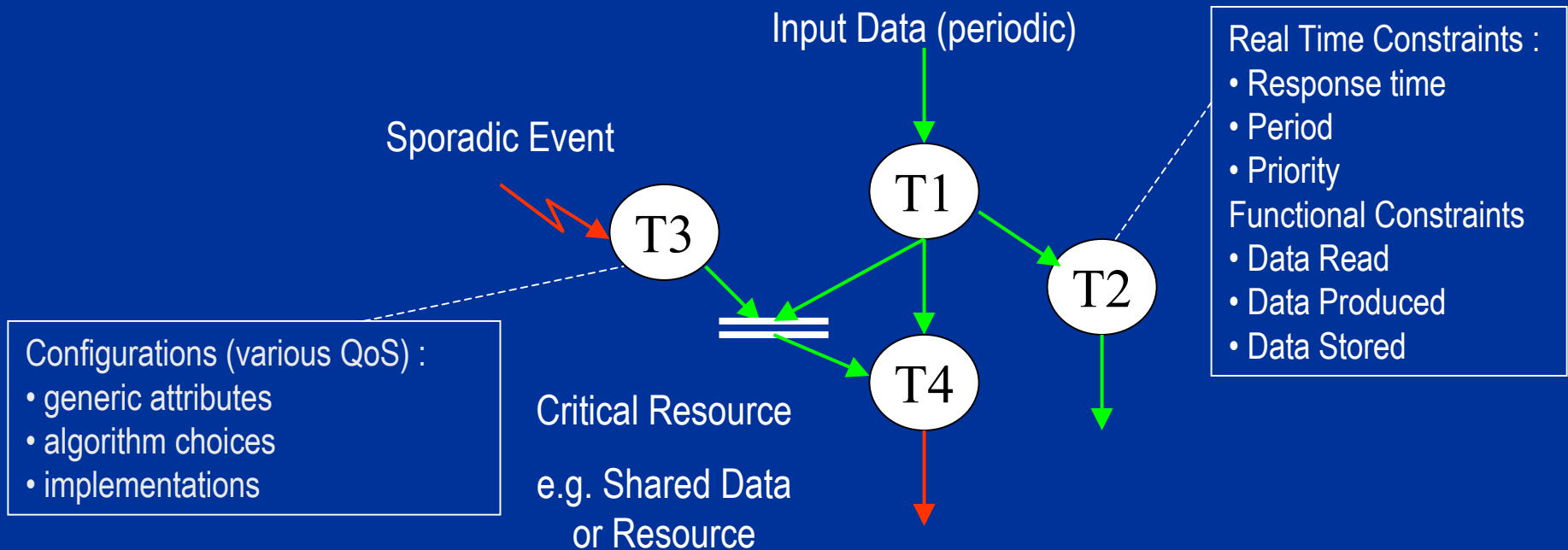
System Modeling

- Event-based / Data-Flow separation :
 - Separate Event Based / Data Flow (Natural Decomposition)
 - Data Flow models : don't fit with Data/Control dependency
 - Event based models : not adapted for Data-Flow parallelism exploration
 - Designer Decisions based on existing designs / Spec / Libraries



System Modeling

- 1st Level, Task Graph :

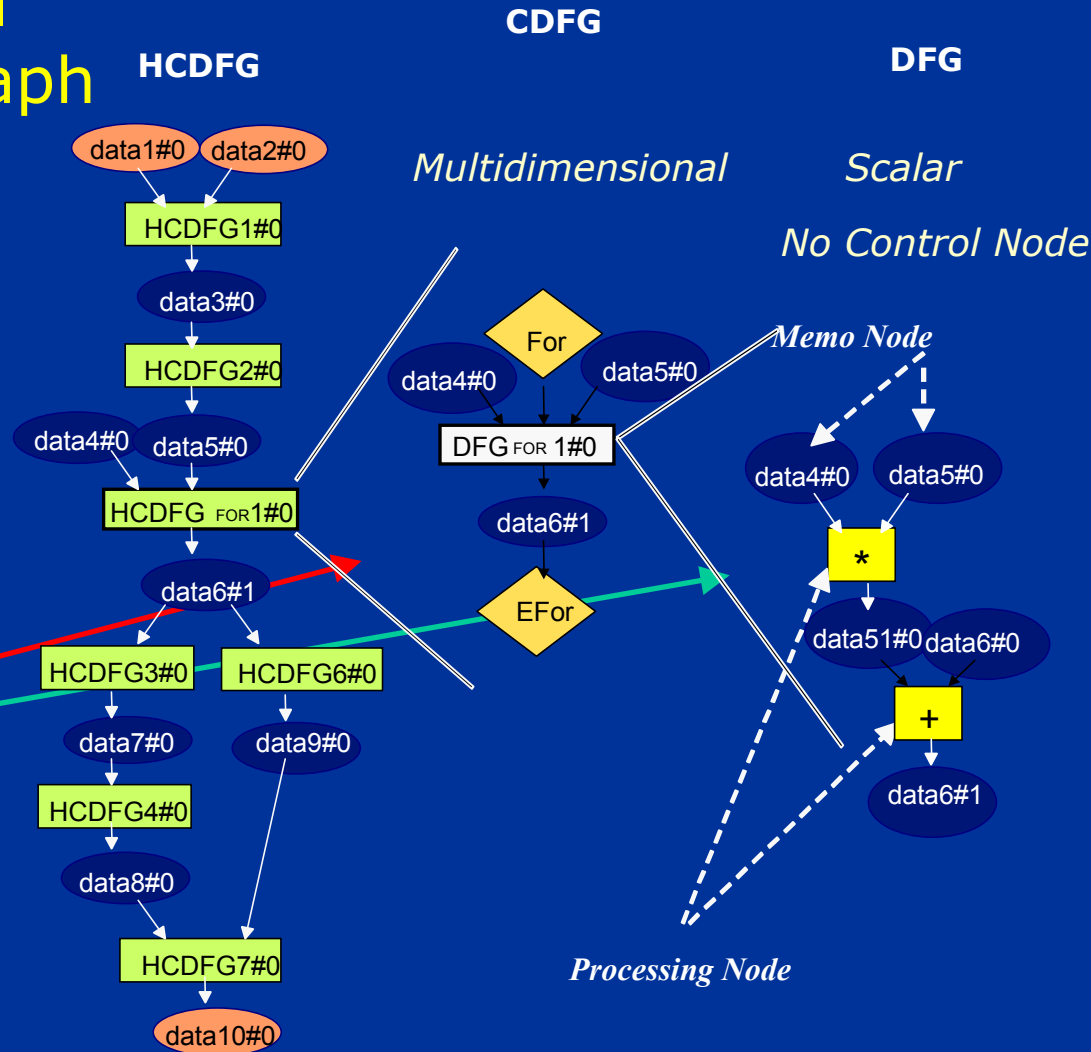


System Modeling

● 2nd Level, Hierarchical Control Data Flow Graph

```
Void function(short data1, short data2, short *data10)
```

```
{
  int i;
  short *data3, *data5, *data6, *data7, *data8, *data9;
  short data51;
  short data4[6]={128, 14, 56, 78, 32, 2};
  subfunction1(data1, data2, &data3);
  if (data3<0) data5 = 0;
  else      data5 = data3;
  for(i=0; i<6; i++)
    data6+=data5*data4[i];
  subfunction3(*data6, &data7);
  subfunction4(*data7, &data8);
  subfunction6(*data6, &data9);
  subfunction7(*data8, *data9, &data10);
}
```



Exploration & Decision Tools I

- Design Trotter - HCDFG Level
 - Fast exploration of architectural implementations
 - Hierarchical Exploration :
 - Different levels of granularity (DFG, CDFG, HCDFG₁, ..., HCDFG_N)
 - Guidance Metrics
 - Tests, Data transfer, Data processing, Parallelism
 - Resource / Delay estimation by Scheduling & Allocation
 - Selection of existing IP (associated to pre-characterized HCDFG)
 - Provide the Partitioning / RT-Scheduling tool with task implementation alternatives

Exploration & Decision Tools I

- **HCDFG-DT Philosophy :**

- 1st Abstraction : Exploration independent from any target
- 2nd Customizable : Mapping of a given parallelism over a given target
- Principle :

HCDFG

=> *A function exists in LIB for that HCDFG ?*

Yes : Get the Solution TradeOff Curve

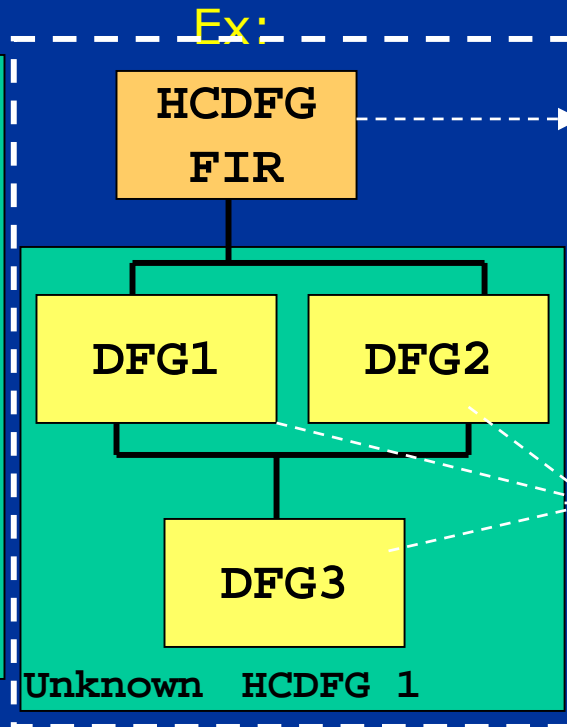
No :

=> **Is-it a DFG ?**

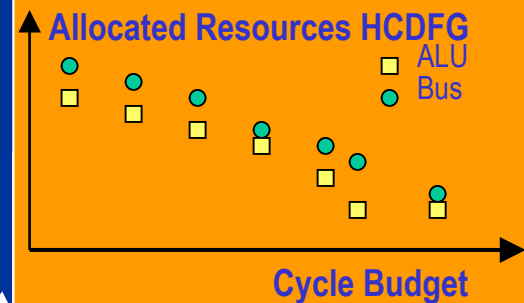
Yes Launch Schedulings

No :Go down to the next Hierarchy Level

If all graphs Traveled :
Combine Results

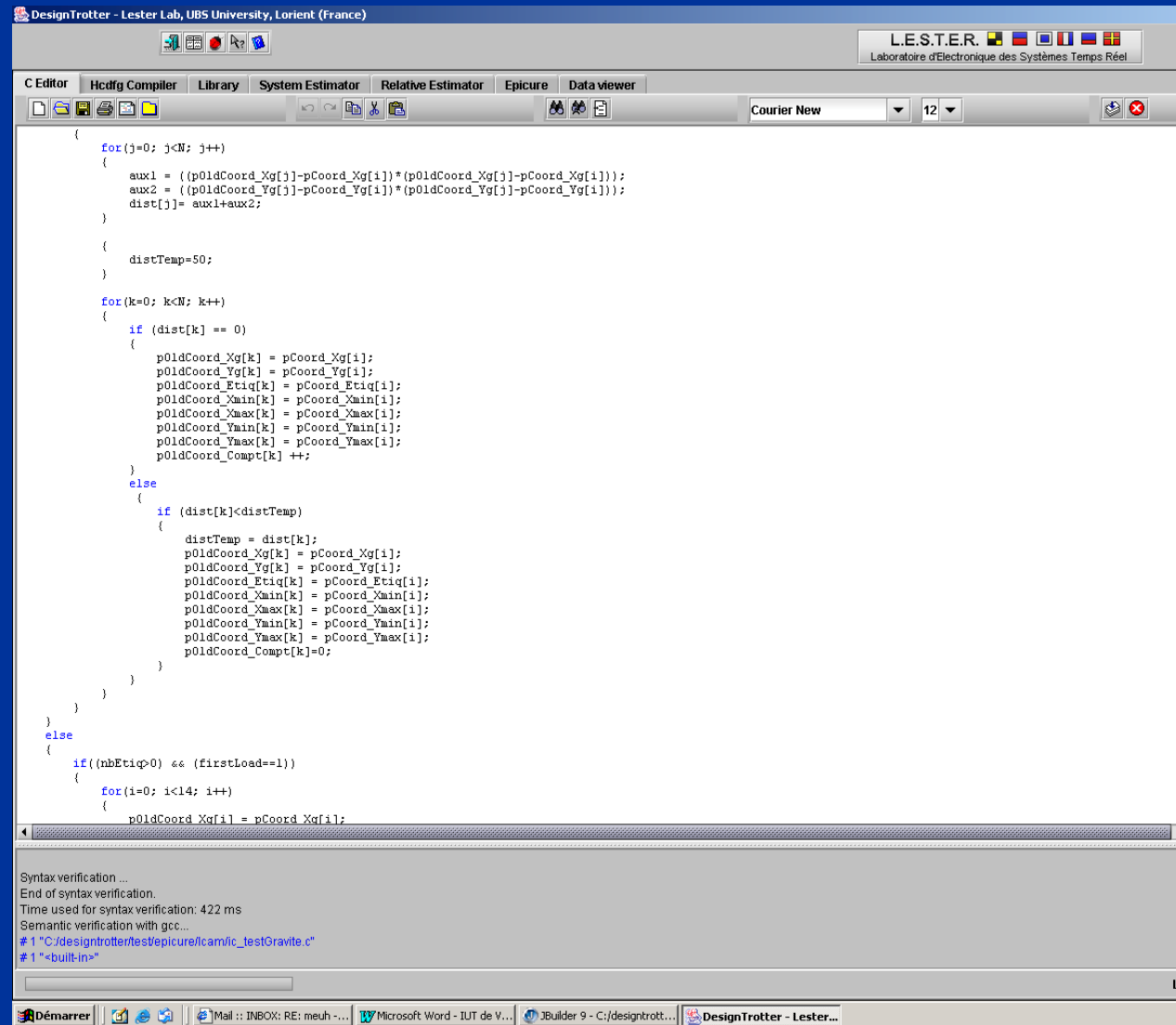


Top results after HCDFG FIR and HCDFG-1 combination



Exploration & Decision Tools I

- A)
 - C Specification
 - Syntax checking
 - HCDFG grammar translation



```
DesignTrotter - Lester Lab, UBS University, Lorient (France)
L.E.S.T.E.R.
Laboratoire d'Electronique des Systemes Temps Reel

C Editor  Hcdrg Compiler  Library  System Estimator  Relative Estimator  Epicure  Data viewer
Courier New  12

{
  for(j=0; j<N; j++)
  {
    aux1 = ((pOldCoord_Xg[j]-pCoord_Xg[i])*(pOldCoord_Xg[j]-pCoord_Xg[i]));
    aux2 = ((pOldCoord_Yg[j]-pCoord_Yg[i])*(pOldCoord_Yg[j]-pCoord_Yg[i]));
    dist[j]= aux1+aux2;
  }

  {
    distTemp=50;
  }

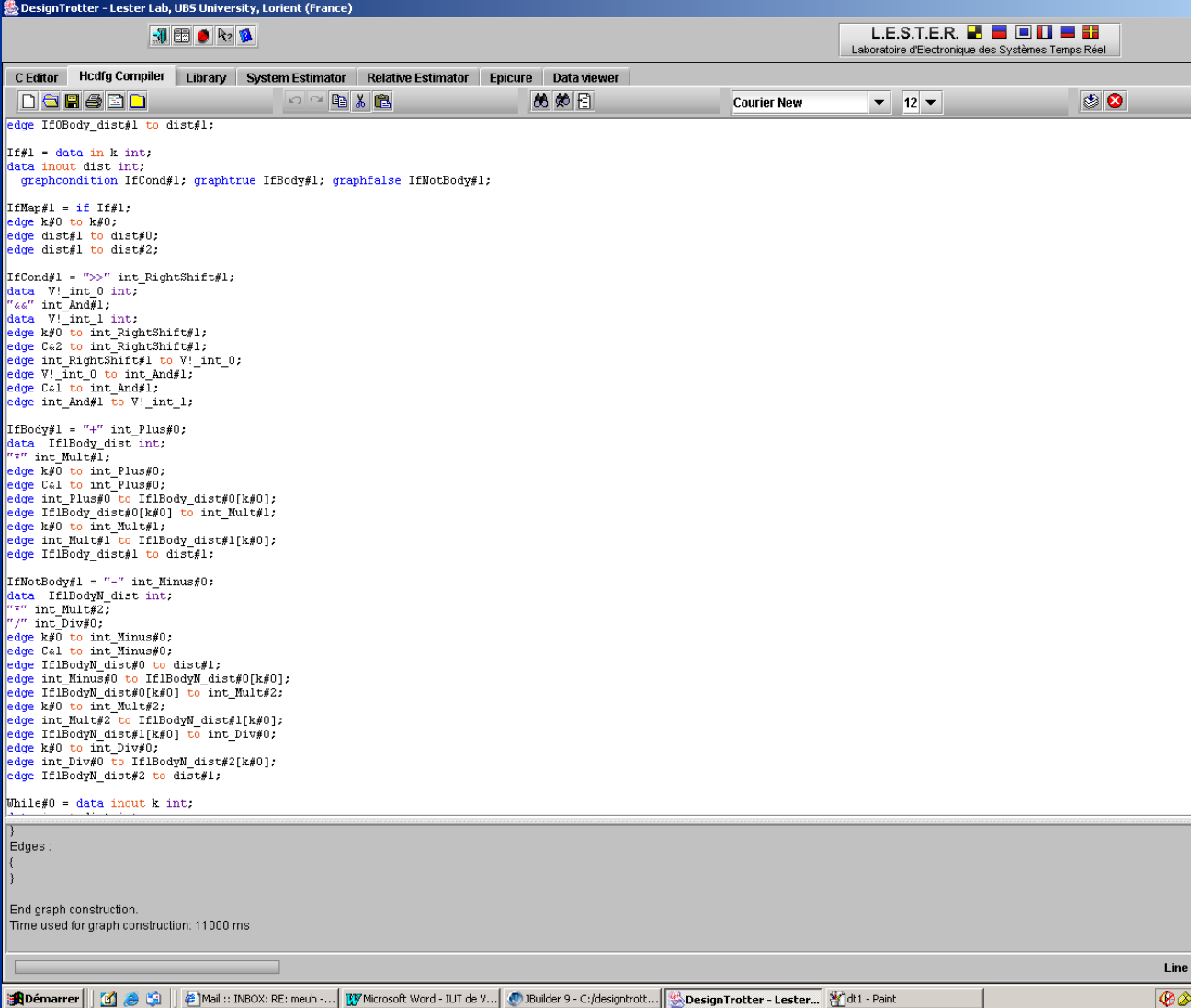
  for(k=0; k<N; k++)
  {
    if (dist[k] == 0)
    {
      pOldCoord_Xg[k] = pCoord_Xg[i];
      pOldCoord_Yg[k] = pCoord_Yg[i];
      pOldCoord_Etiq[k] = pCoord_Etiq[i];
      pOldCoord_Xmin[k] = pCoord_Xmin[i];
      pOldCoord_Xmax[k] = pCoord_Xmax[i];
      pOldCoord_Ymin[k] = pCoord_Ymin[i];
      pOldCoord_Ymax[k] = pCoord_Ymax[i];
      pOldCoord_Compt[k] ++;
    }
    else
    {
      if (dist[k]<distTemp)
      {
        distTemp = dist[k];
        pOldCoord_Xg[k] = pCoord_Xg[i];
        pOldCoord_Yg[k] = pCoord_Yg[i];
        pOldCoord_Etiq[k] = pCoord_Etiq[i];
        pOldCoord_Xmin[k] = pCoord_Xmin[i];
        pOldCoord_Xmax[k] = pCoord_Xmax[i];
        pOldCoord_Ymin[k] = pCoord_Ymin[i];
        pOldCoord_Ymax[k] = pCoord_Ymax[i];
        pOldCoord_Compt[k]=0;
      }
    }
  }
}
else
{
  if((nbEtiq>0) && (firstLoad==1))
  {
    for(i=0; i<14; i++)
    {
      pOldCoord_Xg[i] = pCoord_Xg[i];
    }
  }
}

Syntax verification ...
End of syntax verification.
Time used for syntax verification: 422 ms
Semantic verification with gcc...
#1 "C:/designtrotter/test/epicure/ICam/IC_testGravite.c"
#1 "**built-in**"

Démarrer  Mail :: INBOX: RE: meuh -...  Microsoft Word - IUT de V...  JBuilder 9 - C:/designtrott...  DesignTrotter - Lester...
```

Exploration & Decision Tools I

- B)
 - HCDG file compilation
 - Internal Data Structure Generation



The screenshot shows the DesignTrotter software interface. The title bar reads "DesignTrotter - Lester Lab, UBS University, Lorient (France)". The menu bar includes "C Editor", "Hcdg Compiler", "Library", "System Estimator", "Relative Estimator", "Epicure", and "Data viewer". The toolbar shows various icons for file operations and editing. The main text area contains HCDG code for compiling an internal data structure. The code defines nodes for integers, conditions, and bodies, and edges representing relationships between them. It includes sections for "IfMap", "IfCond", "IfBody", and "IfNotBody". At the bottom, it shows "Edges:" and "End graph construction. Time used for graph construction: 11000 ms". The taskbar at the bottom shows several open applications: Démarrer, Mail, Microsoft Word, JBuilder 9, DesignTrotter, and Paint.

```
edge If0Body_dist#1 to dist#1;

If#1 = data in k int;
data inout dist int;
  graphcondition IfCond#1; graphtrue IfBody#1; graphfalse IfNotBody#1;

IfMap#1 = if If#1;
edge k#0 to k#0;
edge dist#1 to dist#0;
edge dist#1 to dist#2;

IfCond#1 = ">>" int_RightShift#1;
data V!_int_0 int;
" &&" int_And#1;
data V!_int_1 int;
edge k#0 to int_RightShift#1;
edge C&2 to int_RightShift#1;
edge int_RightShift#1 to V!_int_0;
edge V!_int_0 to int_And#1;
edge C&1 to int_And#1;
edge int_And#1 to V!_int_1;

IfBody#1 = "+" int_Plus#0;
data If1Body_dist int;
" * " int_Mult#1;
edge k#0 to int_Plus#0;
edge C&1 to int_Plus#0;
edge int_Plus#0 to If1Body_dist#0[k#0];
edge If1Body_dist#0[k#0] to int_Mult#1;
edge k#0 to int_Mult#1;
edge int_Mult#1 to If1Body_dist#1[k#0];
edge If1Body_dist#1 to dist#1;

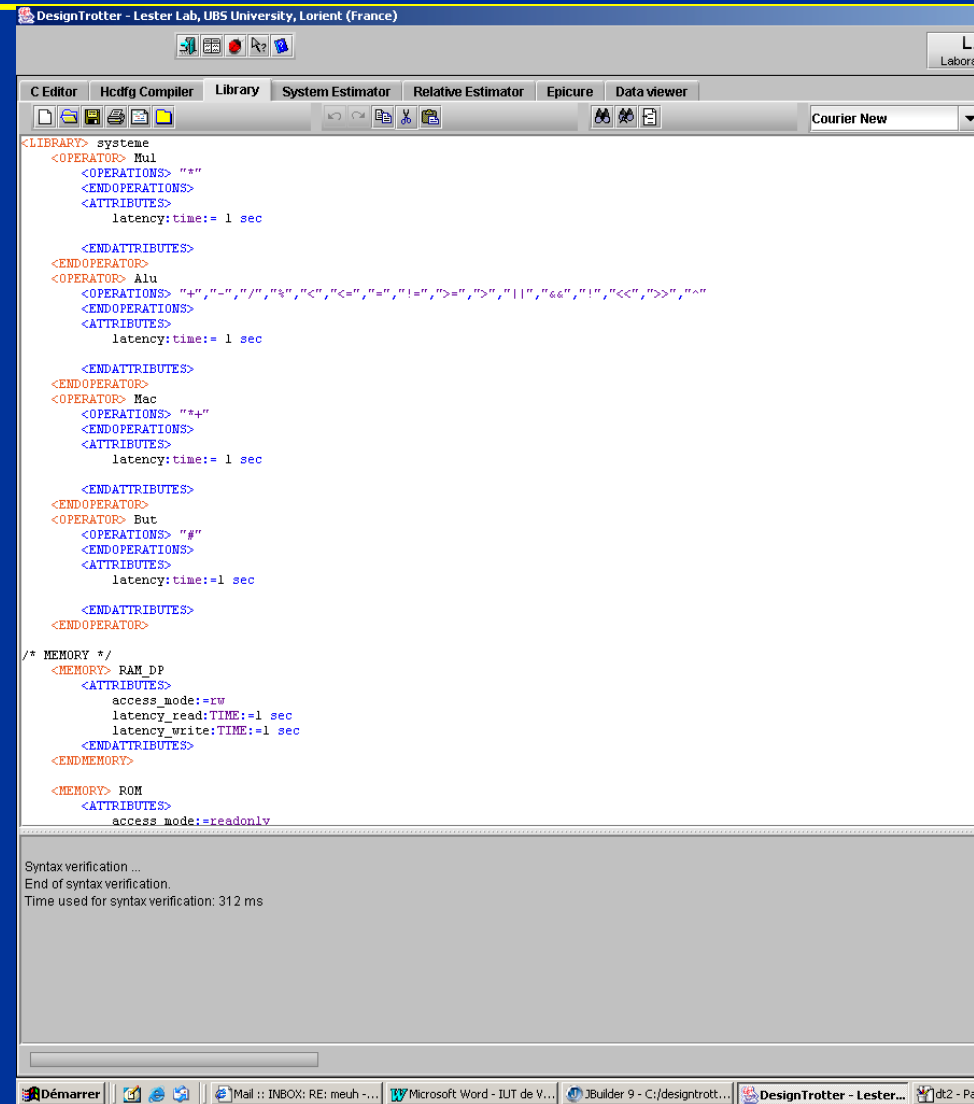
IfNotBody#1 = "-" int_Minus#0;
data If1BodyM_dist int;
" = " int_Mult#2;
" / " int_Div#0;
edge k#0 to int_Minus#0;
edge C&1 to int_Minus#0;
edge If1BodyM_dist#0 to dist#1;
edge int_Minus#0 to If1BodyM_dist#0[k#0];
edge If1BodyM_dist#0[k#0] to int_Mult#2;
edge k#0 to int_Mult#2;
edge int_Mult#2 to If1BodyM_dist#1[k#0];
edge If1BodyM_dist#1[k#0] to int_Div#0;
edge k#0 to int_Div#0;
edge int_Div#0 to If1BodyM_dist#2[k#0];
edge If1BodyM_dist#2 to dist#1;

While#0 = data inout k int;
}
Edges :
{
}

End graph construction.
Time used for graph construction: 11000 ms
```

Exploration & Decision Tools I

- C)
 - Architecture Library Specification
 - Association Operation / Resource
 - Different levels of granularity: possibility to affect a given pre-characterized IP to an HCDFG
 - Without any information : System Level Lib.



The screenshot shows the DesignTrotter software interface. The title bar reads "DesignTrotter - Lester Lab, UBS University, Lorient (France)". The menu bar includes "C Editor", "Hcdfg Compiler", "Library", "System Estimator", "Relative Estimator", "Epicure", and "Data viewer". The main window displays an XML-like library specification for a system named "systeme". The specification defines several operators: Mul, Alu, Mac, and But, each with its own set of operations and attributes like latency. It also defines two memory blocks: RAM_DP and ROM, with their respective access modes and latencies. At the bottom, a status bar indicates "Syntax verification... End of syntax verification. Time used for syntax verification: 312 ms".

```
<LIBRARY> systeme
<OPERATOR> Mul
<OPERATIONS> "*"
<ENDOPERATIONS>
<ATTRIBUTES>
  latency:time:= 1 sec
<ENDATTRIBUTES>
<ENDOPERATOR>
<OPERATOR> Alu
<OPERATIONS> "+", "-", "/", "*", "<", "<=", "=", "!", ">", ">=", "||", "&&", "!", "<<", ">>", "&"
<ENDOPERATIONS>
<ATTRIBUTES>
  latency:time:= 1 sec
<ENDATTRIBUTES>
<ENDOPERATOR>
<OPERATOR> Mac
<OPERATIONS> "*"
<ENDOPERATIONS>
<ATTRIBUTES>
  latency:time:= 1 sec
<ENDATTRIBUTES>
<ENDOPERATOR>
<OPERATOR> But
<OPERATIONS> "&"
<ENDOPERATIONS>
<ATTRIBUTES>
  latency:time:=1 sec
<ENDATTRIBUTES>
<ENDOPERATOR>
/* MEMORY */
<MEMORY> RAM_DP
<ATTRIBUTES>
  access_mode:=rw
  latency_read:TIME:=1 sec
  latency_write:TIME:=1 sec
<ENDATTRIBUTES>
<ENDMEMORY>
<MEMORY> ROM
<ATTRIBUTES>
  access_mode:=readonly
```

Exploration & Decision Tools I

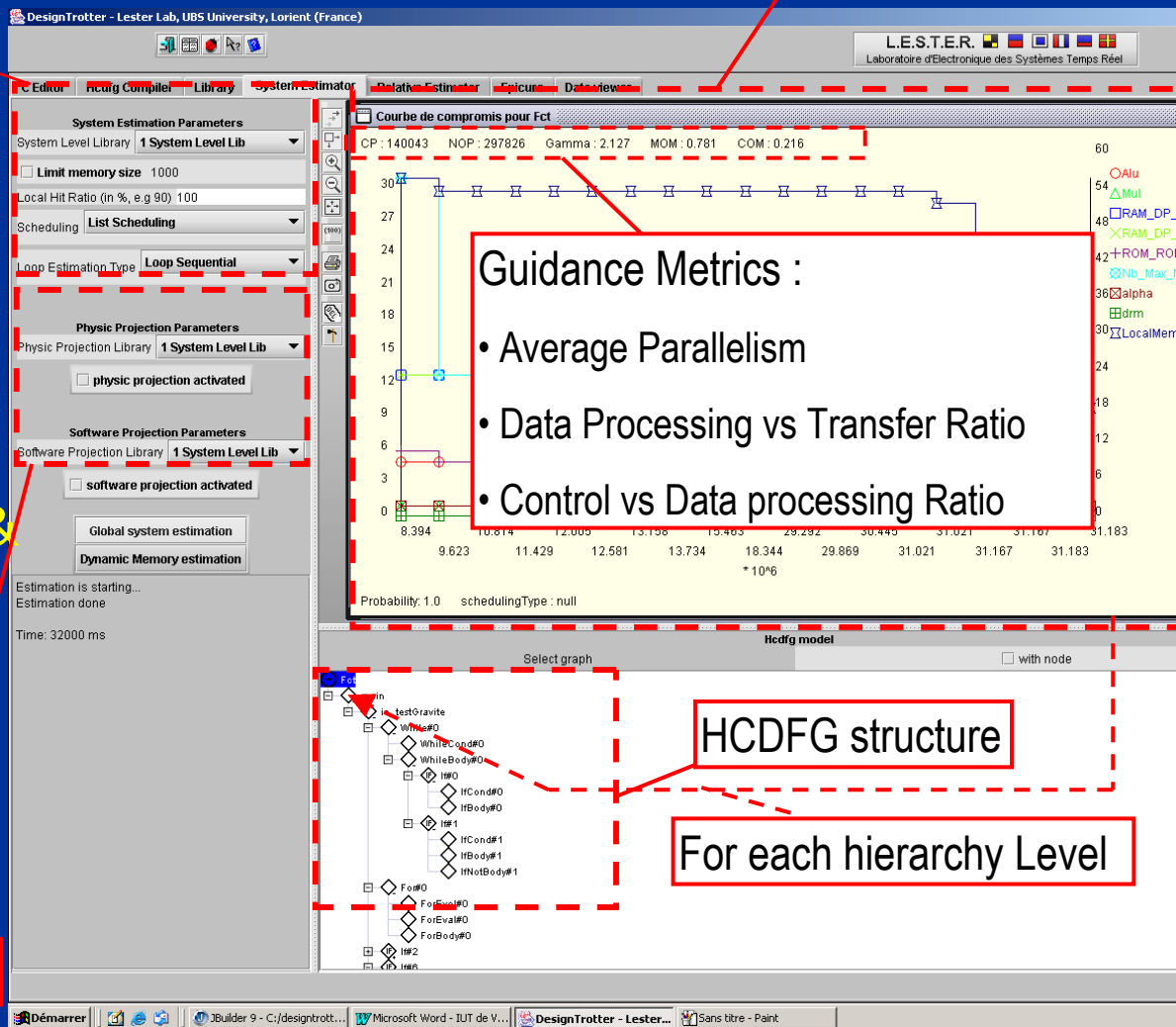
Results : Resource vs cycle budget Trade off curves

Exploration parameters

D)

- Estimation / Exploration
- For each Delay Constraint T :
Critical Path $< T <$ Sequential Execution
- Scheduling of DFGs & combinations to provide Resource vs Cycle Budget tradeoffs

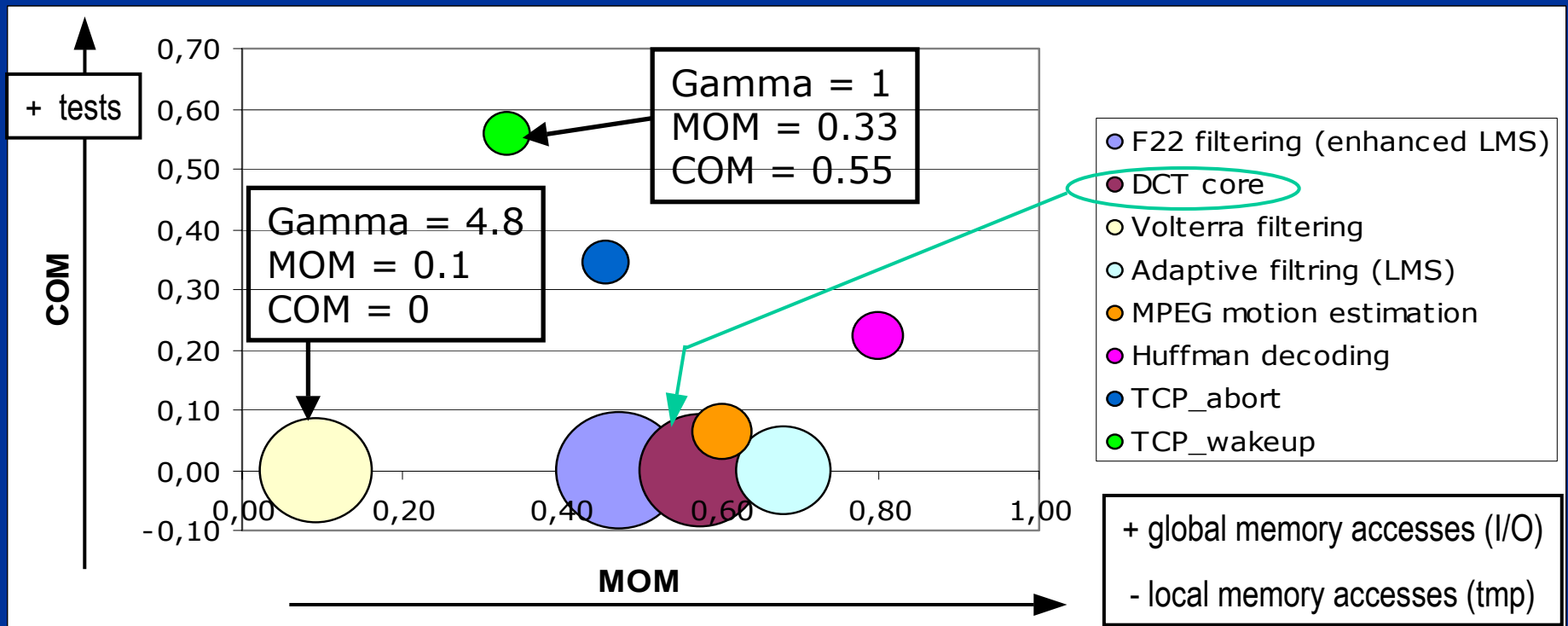
Library selection for archi. projection



HCDFG structure
For each hierarchy Level

Exploration & Decision Tools I

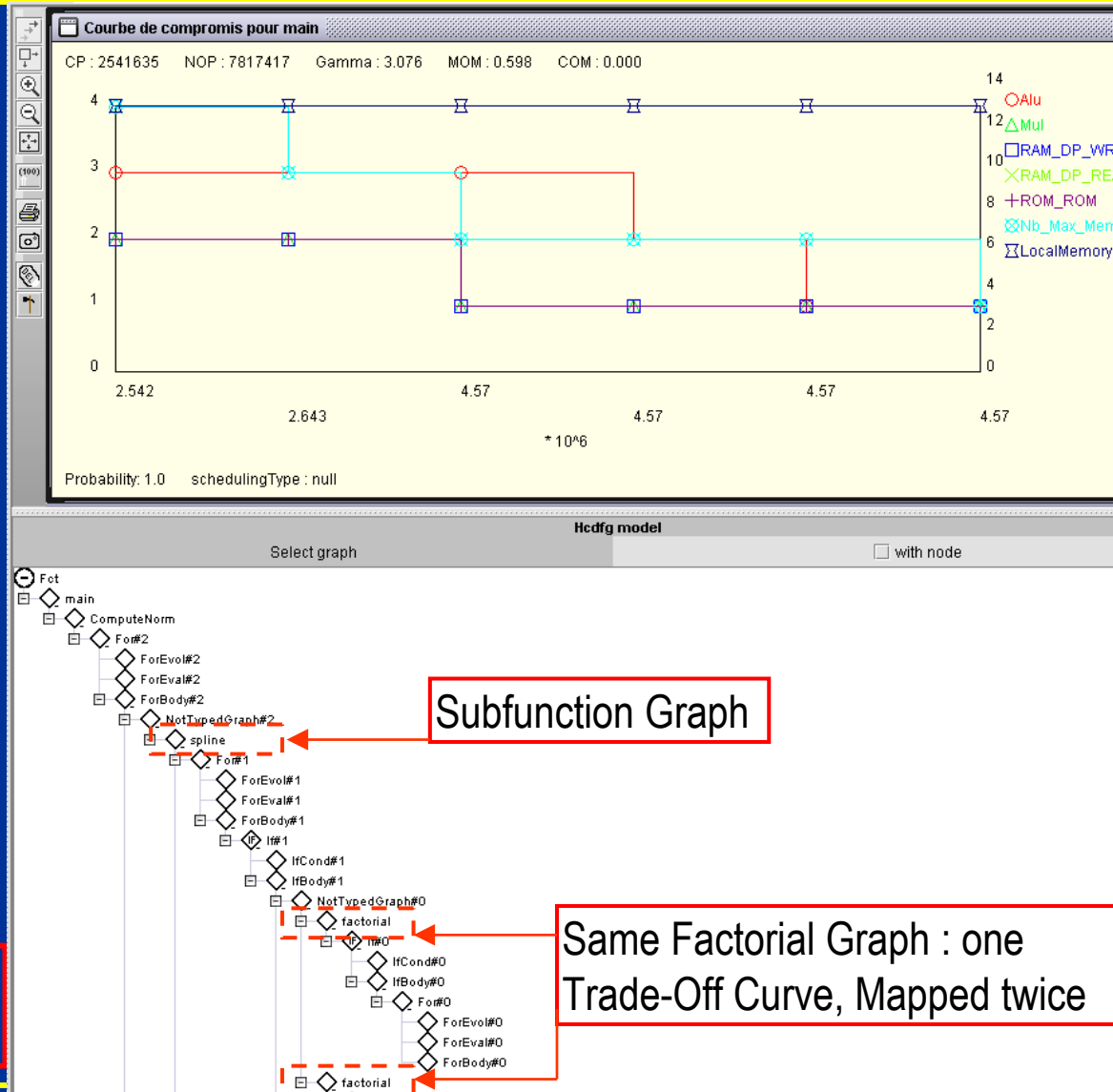
- E.g. Metrics : to quantify the efficiency of allocated resources :
 - Test dominated => GPP (soft real time), FSM HW Block (hard real time)
 - Data-Flow oriented (high γ) => DSP (low MOM), Reconfigurable HW (ad hoc bandwidth)



Exploration & Decision Tools I

- D)
 - Estimation / Exploration
 - Principle => Graph Pattern to be reused and mapped
 - e.g. C Function == Reusable HCDFG

Function Compute Norm from Matching Pursuit Video Coding (EPFL)

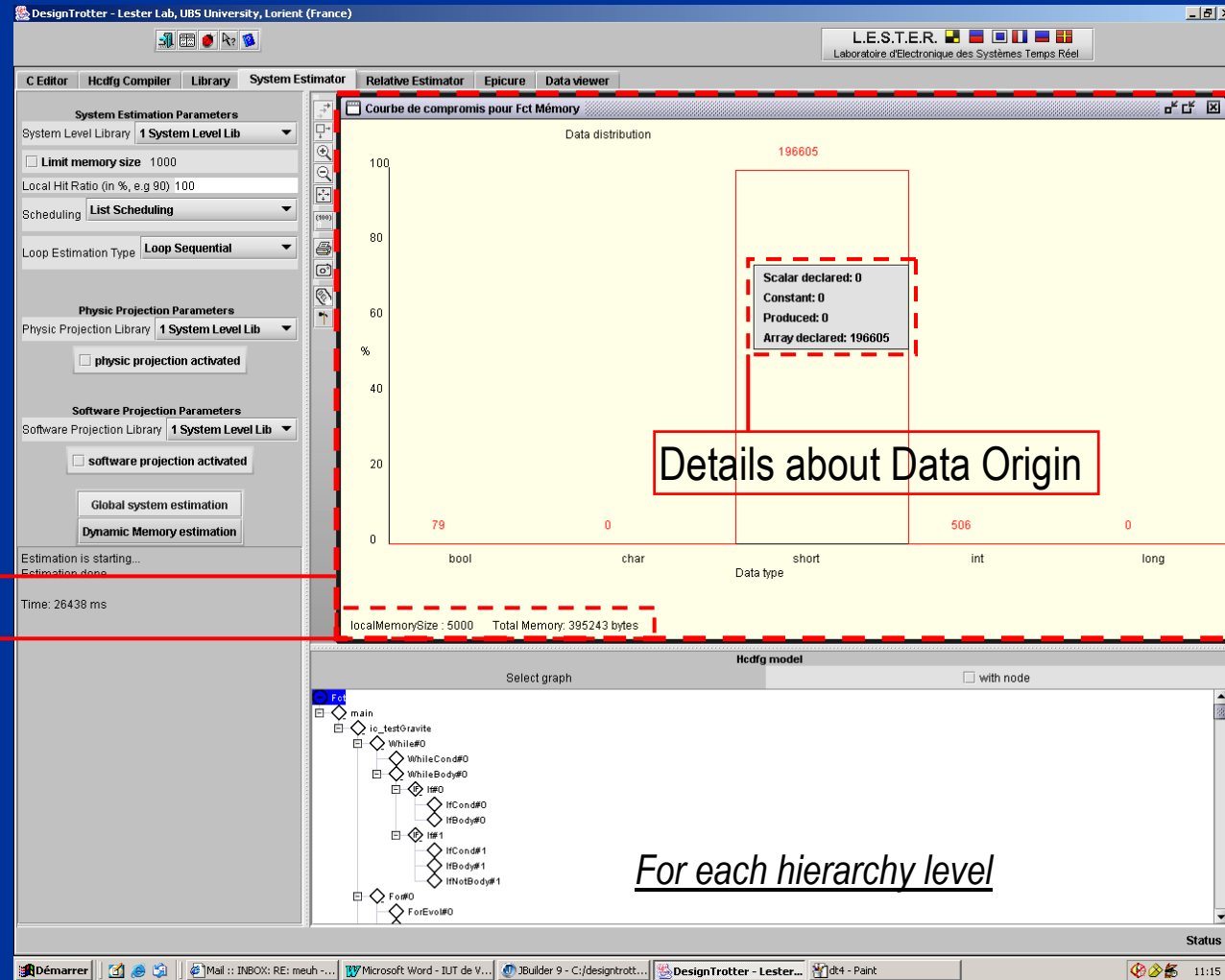


Exploration & Decision Tools I

- E)
 - CAD means a tool to be control by designers => interactivity and Analysis facilities
 - Data Distribution

Data Type Distribution

Local (from Scheduling) & Global Memory Sizes (declared)



Exploration & Decision Tools I

E)

- Complementary analysis facilities :
- Resource / Delay traces from HCDFG down to DFGs

The screenshot displays the DesignTrotter interface with several trade-off curves and a scheduling DFG solution. The curves show the relationship between CP (Cycles Per Instruction), Gamma, MOM (Maximum Overhead Metric), and COM (Cost of Memory) for different components like If#2, IfCond#2, IfNotBody#2, and For#1. The scheduling DFG solution shows resource allocation over cycles.

Associated Scheduling DFG solution

Cycles	Resource 1	Resource 2	Resource 3	Resource 4
0	nl_READ #0%0	ncCore2_READ #0%0	nl_Minus #9	ncSsBord_WRITE #1
1	nl_READ #0%0	ncCore2_READ #0%0	nl_Minus #9	ncSsBord_WRITE #1
2	nl_READ #0%0	ncCore2_READ #0%0	nl_Minus #9	ncSsBord_WRITE #1
3	nl_READ #0%0	ncCore2_READ #0%0	nl_Minus #9	ncSsBord_WRITE #1

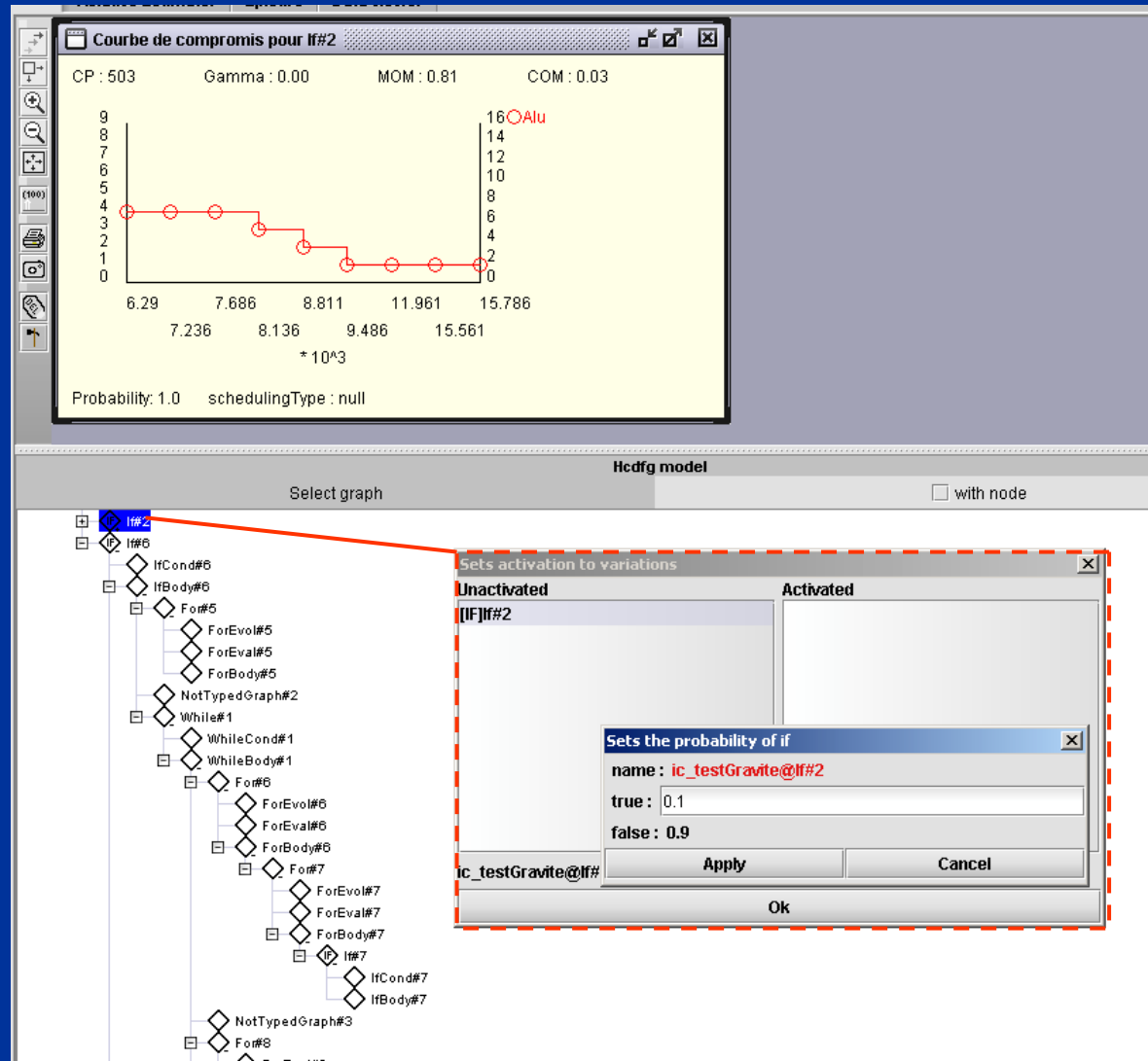
1st a given considered implementa

A particular T = 8136 c which delay allocated to its sub-graphs ?

The Tool provides the links towards the relative solutions at lower levels

Exploration & Decision Tools I

- E)
 - Complementary analysis facilities:
 - Scheduling & Metrics depend on
 - Static Variables:
 - Loop Bounds
 - IF branches probabilities
 - Interactive tool => Values Tuning



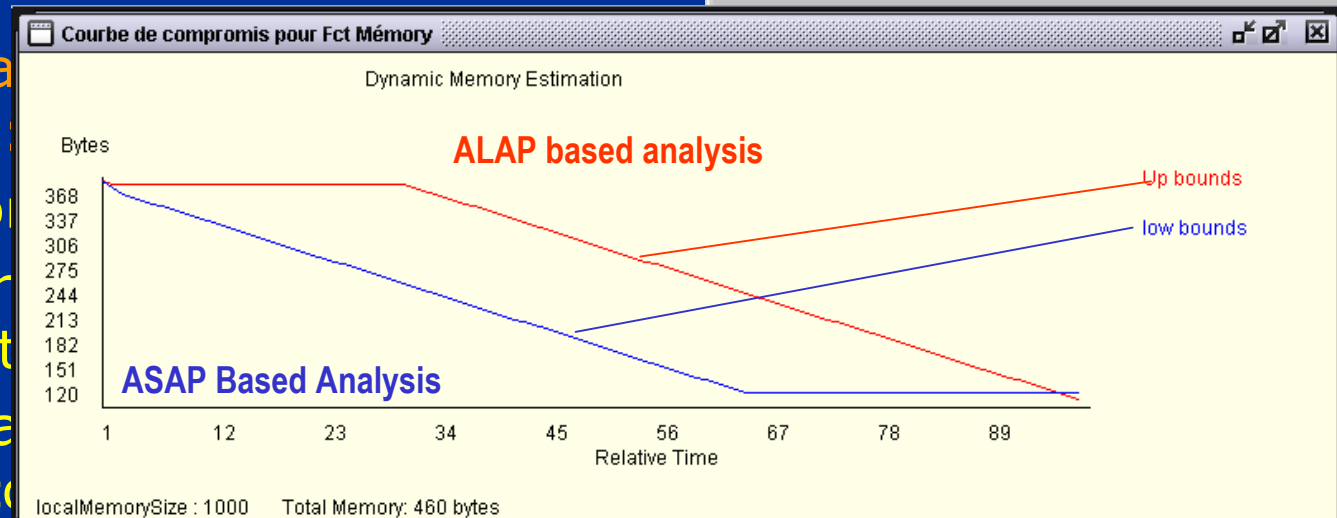
Exploration & Decision Tools I

DesignTrotter - Lester Lab, UBS University, Lorient (France)



● F)

- Dynamic based Estimation
- Main Memory
- Declared Array overestimation
- Memory Trace every time call
- HCDFG-Loop => Iterator Space Model = Polyhedral Data-Flow Graph
- Balasa method (IMEC, INRIA) + DT Hierarchy & Scheduling Methods



```
{  
  b = a[0]+a[1]+a[99];  
}
```

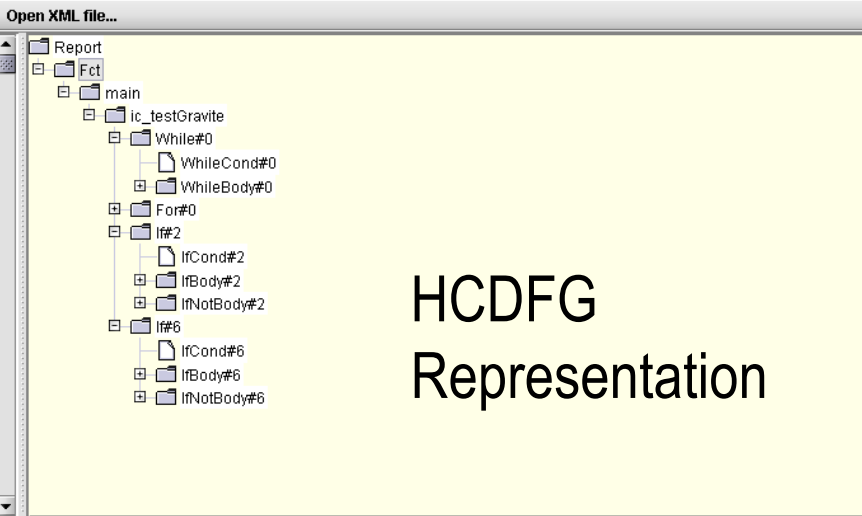
Syntax verification ...
End of syntax verification.
Time used for syntax verification: 375 ms
Semantic verification with gcc...

```

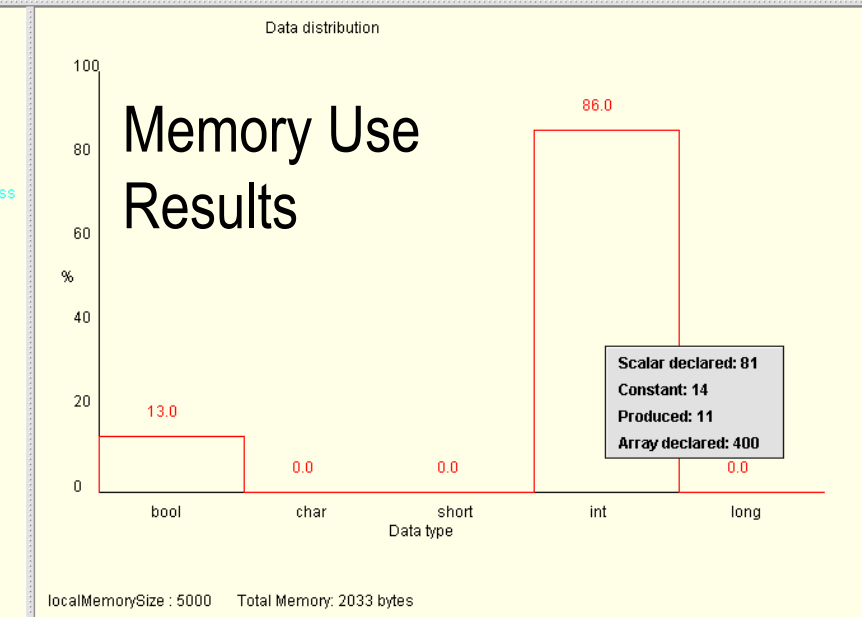
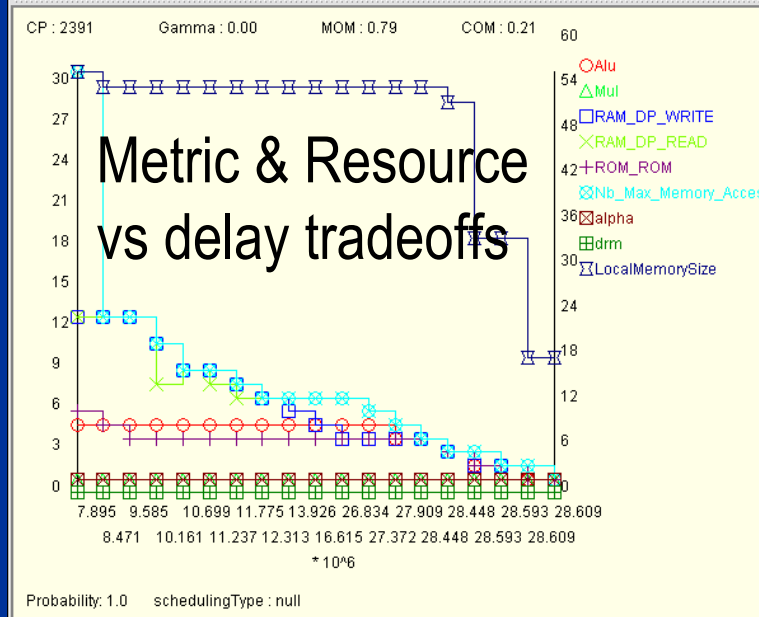
Open XML file...
<?xml version="1.0" encoding="ISO-8859-1"?>
<Rapport>
<Vertex Name="Fct" Type="proxy.reports.VertexData">
<Description>Courbe de compromis pour</Description>
<Probability>1.0</Probability>
<Memory>
<boolean>
<scalarDeclared>15</scalarDeclared>
<constant>0</constant>
<produced>64</produced>
<tableDeclared>0</tableDeclared>
</boolean>
<byte>
<scalarDeclared>0</scalarDeclared>
<constant>0</constant>
<produced>0</produced>
<tableDeclared>0</tableDeclared>
</byte>
<short>
<scalarDeclared>0</scalarDeclared>
<constant>0</constant>
<produced>0</produced>
<tableDeclared>0</tableDeclared>

```

XML data



HCDFG Representation

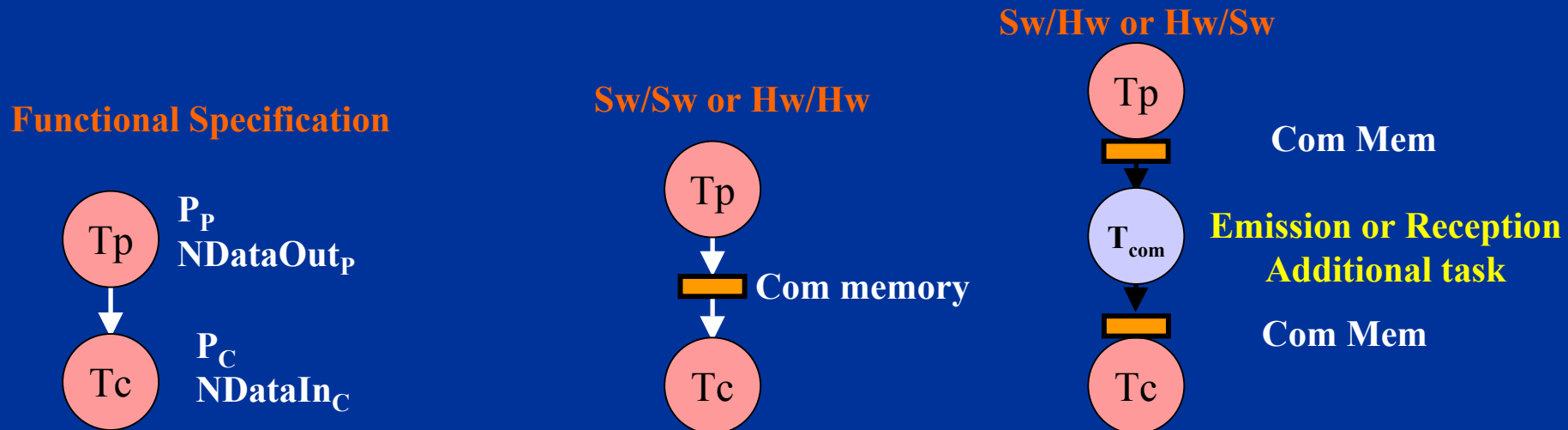


Exploration & Decision Tools II

- Design Trotter : Task Graph Scheduling & Partitioning
 - Problem Inputs :
 - System I/O Real Time Constraints
 - Input / Output Data period
 - Minimum Response Time
 - Minimum Delays Between Subsequent Events
 - Task Implementations Panel From Exploration Step
 - General Purpose Processor + SW Memory
 - DSP + PGM / DATA memory
 - GPP + Coprocessor + SW Memory
 - Dedicated Hardware + I/O Memory
 - Find a Schedulable Solution (meet the deadlines) with Min Cost
 - $Cost = \alpha * (Area) + (1 - \alpha) * (Static \& Dynamic Power)$

Exploration & Decision Tools II

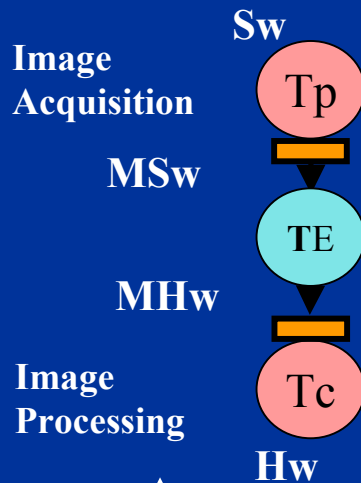
- Real-Time Scheduling with DT :
 - Embedded Systems : fast and small RTOS (e.g. MicroC OS II)
 - Hard Real Time => High Priority First Scheduling
 - Rate Monotonic Analysis (fast, overestimation)
 - And/Or Exact Analysis (slow, accurate including resource sharing, RTOS overhead, etc ...)
 - Soft Real Time => handled by a Server task that gets x% CPU
 - Communication Tasks :



Exploration & Decision Tools II

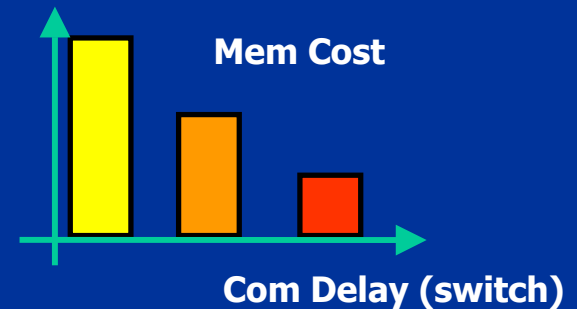
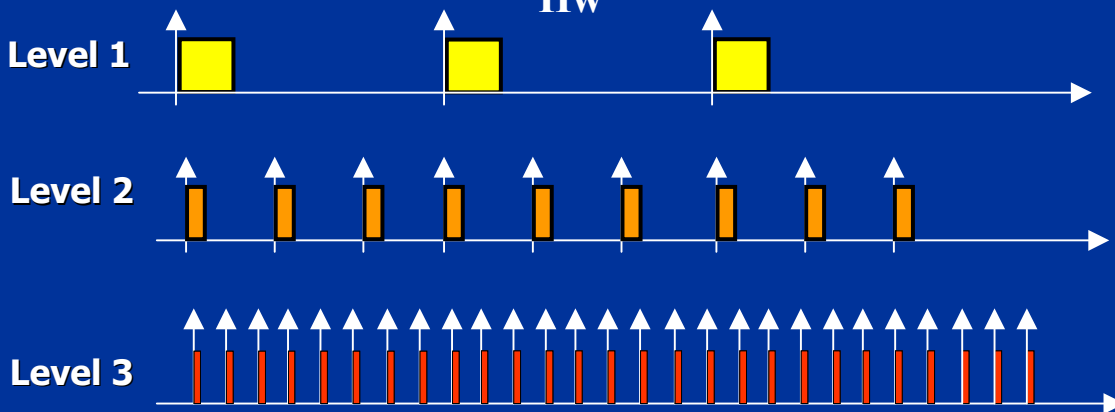
- Hierarchy Level Influence :

- Data transfer and processing Delays delays, and Memory Cost are strongly related to HW Task Granularity Levels :



```

Task Tc loop nest
  For (i=1 to N) {
    For(j=1 to K) {
      ProcessPixel(i;j)
    } Granularity level 3
  } Granularity level 2
} Granularity level 1
    
```



Exploration & Decision Tools II

- Design Space Exploration & HW/SW multi level partitioning
 - Exponential Growth of Design Space with
 - Task Number
 - Implementation Alternatives
 - Two Solutions depending on search space complexity
 - Branch & Bound : Full Search but too slow when task number > 20
 - Simulated Annealing : Heuristic, random search with hill climbing capabilities

Exploration & Decision Tools II

- Design Trotter - TG Tool (1st version) :

Task Graph Specification :

for each task :

- Communications Links (data/control dependencies)
- Implementation Options :
 - SW / COP/ HW
 - Granularity Level
 - Period
 - Cost (Area / Power)

Generic Architecture Specification :

- Mode definitions (V_{dd}, F_{clk})
- Area / Static Power Proc
- etc ...

The screenshot displays the Design Trotter software interface. The main window is titled 'essai' and has two tabs: 'propriétés' and 'Graphique'. The 'Graphique' tab is active, showing a graphical representation of the architecture. A red dashed box highlights an 'OK' button in the 'Modifications de l'architecture?' section. Below this, the 'Exploration' section shows 'Algorithme d'exploration' set to 'Branch and Bound' and 'Nombre de solutions' set to 1. The 'Para' (Parameters) section is visible, showing 'Taux CPU Serveur' and 'Analyse Exacte'. A red dashed box highlights the 'Enregistrer' (Save) button in the 'Fichier' menu. The 'Fichier .cde' window is open, showing the configuration file content:

```
Fichier .cde :
c Estimation et possibilité d'implémentation des tâches du système
n Nom_du_système: Robot
c par l'outil d'estimation système et architectural DesignTrotter
n NmbTache: 18
n NmbCom: 19
(0) Acquisition_vidéo
{
  Implantations Sw 1
  {
    Periode 50000
    DataIn 0
    DataOut 1
    {
      1 65536
    }
  }
  ImpSw 1
  {
    NomPros LEON
    AreaPros 1400 // le coût d'implantation en surface de processeur en us
    PwIdlePros 0.2 // puissance normalisée du processeurs au repos (capacité effective)(ucapacité)
    LargBusPros 32 // 8/16/32 bits
  }
  Bus_de_communication Sw/Hw
  {
    NomBus AMBA
    AreaCost 600 // le coût d'implantation du Bus (us).
    LargBus 32 // 8/16/32 bits
    M0deBus 1 // 1 avec initialisation, 0 sans init
    CylsInit 2 // nombre de cycle d'initialisation
    CylsCom 1 // nombre de cycle pour une Com
  }
  m Modes 2 // le nombre de mode de fonctionnement
  m Mode1
  {
    ClkPro 300 // l'horloge de fonctionnement de processeur uf
    ClkHws 200 // l'horloge de fonctionnement des modules Hws uf
    ClkBus 100 // l'horloge de fonctionnement du bus uf
    VddPro 1.5 // la tension d'alimentation du processeur
    VddHws 1.2 // la tension d'alimentation des modules Hws
    PwOffSw 0.02 // la puissance statique consommée par unité de surface SW (up/us)
    PwOffHw 0.015 // la puissance statique consommée par unité de surface HW (up/us)
  }
  m Mode2
}
```

Exploration & Decision Tools II

- Design Trotter - TG Tool (1st version) :

Exploration Algorithm Selection

essai

propriétés Graphique

Architecture

Modifications de l'architecture? OK

Exploration

Algorithme d'exploration: Branch and Bound

Nombre de solutions :

Paramètres d'ordonnancement

Taux CPU Serveur

Analyse Exacte

Fonction de coût

Area(%) 50

Power(%) 50

Propriétés avancées pour le Recuit Simulé

Entrez vos paramètres

Facteur de décroissance(T°) 0.99

Nombre max d'itérations par T° 10000

Fichier .cde :

```
c Estimation et possibilité d'implémentation des tâches
n Nom du système: Robot
c par l'outil d'estimation système et architectural Des
n NmbTache: 18
n NmbCom: 19
(0) Acquisition_vidéo
{
  Implantations Sw 1
  {
    Periode 50000
    DataIn 0
    DataOut 1
    {
      1 65536
    }
  }
  ImpSw 1
  {
    AreaCost 120
    PwnCost 0.45
    ExeCycles 1000000
  }
}
{
  AreaCost 325
  PwnCost 0.6
  ExeCycles 300000
}
}
(1) Interpolation_de_Bayer
{
  Interpolation_de_Bayer
}
```

RT Scheduling Analysis Method

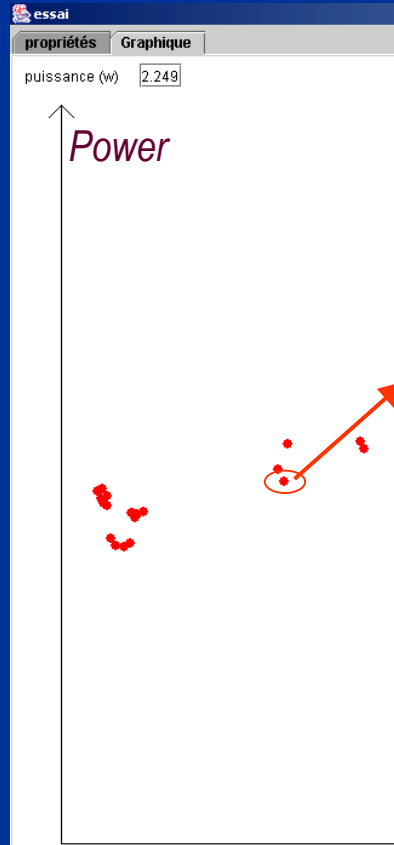
- RM
- RM + Exact Analysis
- Server Task % (Soft Real Time)

Cost Function Tradeoff

- Area / Power Relative Weights

Exploration & Dec

- Design Trotter - TG Tool (1st version) :
 - Tradeoff Curves
 - XML solution description



```
<?xml version="1.0" encoding="UTF-8" ?>
- <fichier_résultat>
- <Informations_système>
  <nombre_de_tâches_d_implantation value="236" />
  <nombre_de_tâches_software value="190" />
  <nombre_de_tâches_coprocesseur value="0" />
  <nombre_de_tâches_hardware value="26" />
  <nombre_de_tâches_d_émission value="6" />
  <nombre_de_tâches_de_réception value="14" />
  <Coût_en_surface value="20993.621 us" />
- <Consommation_du_système value="1.577 W">
  <consommation_statique value="0.62 W" />
  <consommation_dynamique value="0.958 W" />
  <rapport_dynamique_statique value="1.55" />
</Consommation_du_système>
</Informations_système>
- <Informations_logiciel>
  <tension_alimentation_Vdd value="1.8 V" />
  <fréquence_horloge value="450.0 MHz" />
- <coût_en_surface value="18939.82 us">
  <coût_mémoire_tâches value="3680.0 us" />
  <coût_mémoire_tâches_de_com value="150.0 us" />
  <coût_Coprocesseurs value="0.0 us" />
  <coût_processeur_et_bus value="2000.0 us" />
</coût_en_surface>
  <temps_de_switch_sans_cops value="0.0013333333 ms" />
  <temps_de_switch_avec_cops value="0.0013333333 ms" />
- <coût_consommation_partie_software value="1.428 W">
  <coût_consommation_statique value="0.568 W" />
  <coût_consommation_dynamique value="0.86 W" />
  <coût_consommation_dynamique_switch value="0.0010 W" />
  <coût_consommation_processeur_en_Idle value="0.087 W" />
  <rapport_dynamique_statique value="1.51" />
</coût_consommation_partie_software>
- <taux_utilisation_processeur value="0.70089525">
  <taux_utilisation_par_tâche_software value="0.70028836" />
  <taux_utilisation_par_tâche_com value="8.496094E-8" />
  <taux_utilisation_par_switch value="6.068264E-4" />
</taux_utilisation_processeur>
- <tâches_software_coprocesseur>
- <tâches_de_software>
```

Area

- Mode1 (couleur bleue) : tension Vdd Sw = 1.5 V fréquence d'horloge Sw = 300.0 MHz tension Vdd Hw = 1.2 V fréquence du Clk Hw = 200.0 MHz
- Mode2 (couleur rouge) : tension Vdd Sw = 1.8 V fréquence d'horloge Sw = 450.0 MHz tension Vdd Hw = 1.5 V fréquence du Clk Hw = 300.0 MHz

Conclusion

- Promising Work has been done and still remains
 - Main difficulty : in depth **Design & Application Knowledge** required
- HCDFG-DT => links between processor models & resources allocations need to be refined :
 - 1st Improve UAR library definition for existing GPP, DSP
 - Then Power Estimation to be Included and Enforced by Control and Hierarchy HCDFG Model
 - ➔ **Collaborations around specific architectures modeling (e.g. DSP)**
- RT-DT :
 - Static management (engineering)
 - Dynamic QoS Management => a 3 years program is starting (Government Funds for Research, 2 PhD Thesis and positions for master students)
 - ➔ **Collaboration around Case Studies are required to tune and proof approach efficiency (e.g. Mobile Communication & Multimedia Applications)**

PhD Involved in the project

- Former

- Sébastien Bilavarn (Post Doc within EPFL/INTEL Switzerland/USA)
- Yannick Le Moullec (Post Doc within CISS Denmark)
- Azzedine Abdenour (Post Doc within University of Montréal Quebec)
- Lilian Bossuet (Assistant Professor LESTER UBS)

- Current

- Nader Ben Amor (PhD ENIS/LESTER Tunisia/France)
- Issam Maalej (PhD ENIS/LESTER Tunisia/France)
- Yassine Aoudni (PhD ENIS/LESTER Tunisia/France)
- Hédi Tmar (PhD ENIS/LESTER Tunisia/France)
- Samuel Rouxel (PhD LESTER)
- Samuel Evain (PhD LESTER)
- Yvan Eustache (PhD LESTER)

Thank You

Contact:

jean-philippe.diguet@univ-ubs.fr

guy.gogniat@univ-ubs.fr

jean-luc.philippe@univ-ubs.fr

<http://lester.univ-ubs.fr>