Managing Dynamic Partial Reconfiguration on Embedded SDR Platforms

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• Configuration management
• Multi-standards processing architecture
• SDR platform architecture
• FPGA partial reconfiguration
• Conclusion
• Configuration management

• Multi-standards processing architecture

• SDR platform architecture

• FPGA partial reconfiguration

• Conclusion
• SDR multi-standard terminal architecture

Classical approach:
Multiple architecture for multiple standards

Terminal with duplicated HW for each standard

Software-Defined Radio approach:
Single architecture for multiple standards

Terminal with a common configurable computing architecture for all standards
• Our view of configuration management PHY

  – Goals
    – adapt signal processing functionality to the radio application needs
    – perform reconfiguration over heterogeneous computing resources
    – control the reconfiguration process
  – Constraint
    – run-time reconfiguration requirements
- Configuration management units (CMU): distributed over processing blocks

- Different kinds of CMU
  - processing nature
  - underlying hardware
  - depth of reconfiguration
• Expected scenarios
  – standard changing
  – mode changing
  – service changing
  – performance enhancement
  – bug fixing
• Identified constraints for SDR
  – distributed management
  – multi-granularity issue
  – in function of the HW support

L1_CM :
  – Global manager
  – Standard parameter control
  – Dispatches orders to lower layers

L2_CMUs :
  – Function Level
  – Independent of the HW
  – Manages several elementary PB-processing blocks of lower granul.

L3_CMUs :
  – Processing blocks configuration
  – Embedded very closely to the PB
  – Dedicated to the nature of reconfigurable resources
- Configuration management
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• Baseband transmitter chain
  – GSM (Voice, mono carrier)
  – UMTS (Data, High Mobility, CDMA)
  – 802.11g OFDM Mode (High Data rate, multi-carrier)
• Classification of processing functions in 3 classes
  – depending on processing nature

  - Data Structuring Class
    - Memory Intensive
  - Coding Class
    - Flexibility Intensive
  - Modulation Class
    - Computation Intensive

  – deduction of the mapping on 3 clusters HW resources
• Distributed processing
• Heterogeneous processing devices
  – depending on processing nature
  – 3 clusters of HW resources
• Different architecture granularities have to be considered
  – depending on processor and processing nature
  → Very close to configuration management considerations
  → Both can easily be merged in the global SDR system design
- Configuration management
- Multi-standards processing architecture
- SDR platform architecture
- FPGA partial reconfiguration
- Conclusion
• Combine both
  – reconfiguration management - hierarchical
  – data processing - distributed

Configuration management

- L1_CM
  Standard Set

- L2_CMU
  Function Set

- L3_CMU
  Block Set

SDR Processing

- Coding PC
- Data Structuring PC
- Modulation PC

Processing cluster level

- Processing Function level (independent of the HW)
- Processing Blocks level (deployed on the HW)
Hierarchical approach for SDR system Design

- **L1_CM**
  - Standards Parameters Lib.
  - µP

- **L2 CMUs**
  - µP
  - Program Mem.

- **L3 CMUs**
  - µP
  - Cop1
  - DSP
  - Data Mem.

- **Array of BlockRAM**
  - µP
  - DMA
  - Data Structuring Cluster

- **L3 CMUs**
  - µP
  - Core Lib.

- **HW Acc1**
  - DSP
  - Data Mem.

- **Modulation Cluster**
• HW platform composed of 3 processing units
• Heterogeneous processing units

GPP+Memory : host PC
FPGA : Xilinx Virtex II
DSP : TI C64
- Configuration management
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• Partial reconfiguration
  – save reconfiguration time
  – save bandwidth for OTAR by downloading

• FPGA context
  – dissuasive time of total reconfiguration for large FPGA (~100 ms per million gates - Virtex)
  – memory limitations to store total bitstreams
  – control resource savings
    • a plurality of successive designs instead of heavy control state machines
  – permits to modify the structure of a design
• Common operator approach
  – parameters change the operator functionality
  – managed at the L3_CMU level
• FPGA fixed area for management contents
  – Processor CORE (µBlaze/PPC for Xilinx)
  – operators
  – dedicated state machines
• FGPA dynamically reconfigurable area
  – operators parameters (managed by L3_CMU)
  – intra-operator routing (managed by L3_CMU)
  – inter-operator data flow changes (m.b. L2_CMU)
• Module-based design flow on Virtex II devices

• Multi-objects in large FPGAs
• DSP device
  – downloads bitstreams
  – through SelectMap interface
• SRAM
  – bitstream storage
• Configuration management
  – external L2_CMU on DSP
  – L3_CMU wired in the FPGA within or close to operators
• µBlaze
  – Read/write bitstreams
  – into ICAP

• Boot loader
  – if no DSP
  – initial config.
  – instanciates ICAP, µBlaze

• Configuration management
  – internal L2_CMU: µBlaze embedded in the FPGA
  – flexible L3_CMU: µBlaze embedded in the FPGA
  – or/and L3_CMU wired in the FPGA within operators
• Configuration management
• Multi-standards processing architecture
• SDR platform architecture
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• Conclusion
• Multi-level granularity needs for reconfiguration of SDR have been identified
• Hierarchical configuration management to optimize reconfiguration is proposed
• Multi-standard functional architecture model
• Deduction of an SDR architecture applicable to any hardware platform
• Support any partial reconfiguration of the SDR processing chain
• Illustrated by a FPGA partial reconfiguration implementation
Thank you for your attention