## ELECTRONIC SYSTEMS, NETWORKS and IMAGES

Professor in charge: Jacques WEISS

### COURSES

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<th>SUBJECTS</th>
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<td><strong>1 – ELECTRONICS</strong></td>
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<td><strong>2 – ELECTRONIC SYSTEMS</strong></td>
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<td><strong>4 – IMAGES</strong></td>
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<td><strong>7 - END OF STUDIES TRAINING PERIOD</strong></td>
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<td>112,5 h</td>
<td>68 half-days lab works</td>
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WE: written exam
Exam : exam common with several courses (written or oral exam, or presentation)
The aim of the specialization in “Electronic Systems, Networks & Images” is to train highly skilled engineers in electronic systems, especially for nomad and mobile applications.

- Signal processing with case studies for multimedia, digital communications and networks.
- Design of analog and digital electronics: define, in good adequacy between technology and applications, architecture of systems; main performance targets are speed, cost, power consumption, integration density.
- Design management including methods and tools, necessary for engineers to specify, realize, test and qualify industrial products.

A set of topical seminars on state of the art applications, delivered by industrialists, is used to illustrate the use of these techniques in the economic world.

The training is thus designed so as to allow the students to master methods and tools used in current developments, but also to be a driving force for future evolutions in a large industry spectrum.

Electronics

INTEGRATED ANALOG ELECTRONICS
15h C/ 6h BE / 1 exam / 2 ECTS credits SERTIM
Gilles Tourneur (7h30), Christian Moreau (7h30)

Different technological steps: processes and equipment


Technology ways

Bipolar: description of the technology, implementation of NPN and PNP transistors, diodes, resistors and capacitors. MOS: NMOS, CMOS.

Faults, degradation mechanisms and technological improvements


Development of IC technology

Submicron CMOS. BICMOS. Gallium arsenide, silicon on insulator.

Production of integrated circuits


Packaging and Interconnections


Bibliography:

HARDWARE ARCHITECTURES (FPGA and PROCESSORS)
18h C / 9h BE / 1 exam / 2 ECTS credits SERIAM
Pierre Leray (9h), Jacques Weiss (9h)

Microprocessors and associated components, which have been available since the first digital integrated circuits appeared in the early ’70s, now form the core of most electronic products: they are found almost everywhere, particularly in information technology (from pocket calculators to computers), cars (ABS, injection systems, etc), automation equipment (programmable controllers, process control, etc) and domestic appliances (thermometers, remote controls, smart cards, etc).

Programmables devices (FPGA) (4,5 h C)

Programmable components can be used to implement extremely fast arithmetic logic functions in a short development time. Due to technology improvements, it is now possible to integrate processor cores, this introduces the concept of SoPC (System On Programmable Chip).

The aim of this course is to place these programmable components in context with the other means of implementing a given task and to analyse the main architectures available on the market (Actel, Atmel, Altera, Xilinx, etc). After this analysis, student will be able to assess the enhancements provided by the new architectures and find the most suitable component for a given function.
Design approaches and market for programmable components
Criteria for selecting a particular technology: the technical, industrial and economic aspects.

Families of programmable components
From PAL and CPLDs, right through to FPGA: analysis of various architectures and their potential. Development of families and position in relation to the market.

Methodology and design tools
EDA tools.
Introduction to VHDL, description language for digital circuits and systems. Functional analysis and logic synthesis

Use of programmable components
Fields of application (signal processing, digital television, etc). Performance and limitations of the technology. Development systems.

Concept of SoPC (System on Programmable Chip)
Hard and Soft cores, reconfigurable hardware, dynamic reconfiguration

Microprocessors (12h C)
This course present the main architectural concepts used on state-of-the-art general purpose processors with analysis of the optimal adequacy with technology.

Structure and organisation of programmed systems
Central Unit
Memory : technologies and organisation.
Internal and external busses.
Peripheral components.

Processors architectures
RISC, CISC, VLIW and DSP architectures
Performance optimizations
Hierarchy, technology and structure (cache insertion)
Out-of-Order (speculative) sequencing
Branch prediction
Hyper-threading

Multiprocessing
Optimization of arithmetic structures

Bibliography:
Structured Computer organisation, Prentice-Hall.
The cache memory book, Academic press.
Electronic Systems

DIGITAL SYSTEMS DESIGN
18h C / 6h BE / 1 examen / 2 crédits ECTS

Didier Louis (9h), Christophe Moy (3h), Amor Nafkha (3h), études de cas : Bruno Dufrien (3h)

To optimize performances, systems use lasted technologies for chips and packaging

The product may be “System on Chip”(SoC), “System in Package”(SiP) or “System On Board”, in all cases, it is necessary to use adapted methodology et suitable tools from conception to validation.

Introduction :
Electronic market technologies, prices and trends

Design techniques, description and comparison
Methodology and development cycles for board designs
ASIC technologies – Foundry/customer relationship

Design of circuits libraries
From base circuits up to complex functions (IP : Intellectual Property) – integrated memories self-test

System On a Chip

SOC core blocks
Processors cores – buses – reused logic.
The Reuse Methodology Manual.

SOC design
Specification – functional, architectural and hardware design

Memory design
DRAM - SRAM - non volatiles Memories.

Complex systems description and design, trends on design approaches
High-level Description Tools and languages, co-deign ; hardware/software partitioning ; heterogeneous platforms

Design of complex systems, trends of methods
High level digital flow of heterogeneous systems.
SystemC design flow.
Hardware-software partitioning. Cosimulation, modelisation
Abstraction levels (UTF, TF, TLM, RTL, …).

Optimization and Operational research
Graphs theory. Scheduling. Resources allocation. Parallel computing

VALIDATION AND TEST OF ELECTRONIC SYSTEMS
21h C / 1 exam / 1 ECTS credit

Bruno Dufrien (3h), Dominique Guérin (3h), Yann Le Guillou (6h), Jacques Weiss (6h)

System testing is an important aspect of a manufacturer’s strategy. It is used to measure the quality and reliability of products, and thus to validate the entire production sequence. The complexity and performance of systems are constantly increasing, so testing equipment is becoming ever more expensive. As a consequence, design strategies are needed that make testing easier, thus cutting costs. Testing must be carried out at every stage of production (from the integrated component and the printed circuit board, right through to the finished system). The testing equipment and strategies are therefore adapted to suit the particular context; characterization and maintenance also impose specific constraints.

Overview of the instrumentation used
Signal integrity, interconnections characterization, disturbance sources.

Power supply and parasitics rejection
Power supply circuits, specific components, decoupling.

Characterization
Functional verification, characterization and tests. Fault diagnosis and location.

Testing printed circuit boards
Methodology and tools for investigation
AOI (Automated Optical Inspection). In-Circuit test. Functional test. JTAG standard.

Testing integrated circuits
Testing with and without contact. Testing mixed circuits: analog and digital access.

Developments and trends
CAD and testing equipment. How far should the testing go? Development of new design and testing approaches.

Testability
Access limitations on integrated circuits, testability analysis, fault modelling and simulation ; test patterns generation (ATPG) ; DFT : Design For Test.
DIGITAL TRANSMISSIONS
12h C / 6h BE / 1 exam / 1 ECTS credit  SERITNM
Dominique Leroux (7,5h) , Yves Louët (4,5h).

Reliable data transmission in noisy environments requires the use of suitable methods. The aim of this course is to introduce the various digital modulation methods and their performance and to show how the combination of coding and modulation enables transmission performance to be enhanced.

Transmission channels
Wireless (Radio) channels modelling for indoor and outdoor communication. Wired, phone lines and power-line networks.

Digital modulation
Digital modulation principles. Various types of modulation: PAM, QAM, PSK, FSK

Digital demodulation
Principles and methods. Calculation of performance levels in the presence of noise.

Multi-carrier modulations
OFDM (DVB-T/H, ADSL) : Principles ; realization using an FFT operator.
Coded modulation : COFDM.

Spread-spectrum modulations
CDMA (UMTS, WiFi ), choice criteria.

Carrier synchronization

Three case study practices :
- MAQ-16 modulations MAQ-16, error probabilities, comparison with MDP-2, effects of a bad synchronization.
- Simulation of a transmission chain ; study of adapted filters and Nyquist filters.
- OFDM application : DAB (Digital Audio Broadcasting).

Bibliography :

NETWORKS FOR COMMUNICATION AND BROADCAST
9h C / 1 exam / 1 ECTS credit  SERIRCD
Véronique Alanou (4,5h), Eric Deniau (3h), Jacques Weiss (1,5h)

Any specialist in the field of architecture and integration of electronic systems is affected by data networks in two ways – first as the designer of components and equipment and second as a network user (CAD, production, etc). This course describes the architectural concepts of networks, public networks, local area networks and the available services ; media are also concerned such as radio and power-line networks.

Wide Area Networks (WAN)
The ATM protocol : physical, ATM and adaptation layers, signalling – access control methods.
Multi Protocol Label Switching (MPLS) : notions on IP (Internet Protocol), Quality of Service (QoS), VPN.

Protocols and networks SONET/SDH
Network characteristics, OSI reference model, QoS, nodal functions.
PDH/SDH protocols : PDH and SDH Hierarchies, SDH layers, SDH frames, QoS, protection mechanism, SONET/SDH standard

Wireless and mobile phone networks
Network protocols and topology ; structure and frequency planning

Terrestrial Digital TV broadcast for nomad and mobile TV (DTTV & DVB-H)
Broadcast networks protocols and topology ; structure and frequency planning

Bibliography :
H. Nussbaumer, "Téléinformatique", volumes 1 à 4, Presses Polytechniques Romandes.
G. Pujolle, "Les réseaux", Eyrolles
P. Rolin, "Réseaux hauts débits - Réseaux et télécommunications", Hermes.
A. Tanenbaum, "Réseaux", Prentice Hall - InterEditions.
A. Tanenbaum, "Réseaux : Architectures, protocoles, applications", InterEditions.
C. Servin, "Télécoms, de la transmission à l'architecture de réseaux", Collection Systèmes distribués.
Digital processing
Signal digitization. Representation of numbers. Filtering functions (structures and synthesis).

Signal coding basis
Statistical signal properties, predictive and entropic coding (Huffman, Arithmetic, LZW, Golomb).

Adaptive filtering, linear prediction
Time and frequency-related algorithms. Speech processing applications.

Multi-rate processing systems

Transforms (Fourier, DCT, wavelet)

Sound and image compression (MPEG)
Compression of the audio signal in radio communications and digital television (CELP, MUSICAM, Dolby AC3).
Image compression: transformation, quantization, motion estimation and compensation.
International standards : MPEG -1, -2 et -4/AVC, DCI (Digital Cinema)

Neural networks

3D image synthesis
3D models, vertex generation, texturing and fragment shading

Bibliography:
S.J. SOLARI, "Digital Video and Audio Compression", McGRAW-HILL.

Image analysis (filtering, segmentation, pattern recognition)
3D image synthesis
Implementation (graphic accelerators, GPU, GPP, OpenGl, Cuda, Python)
Experimental work

Students will be divided into groups and will carry out laboratory work (long projects lasting 8, 6 and 4 sessions (half-days), for much of which they will be left to work on their own initiative and will be expected to set up, run and interpret the results of their experiments) and an industrial study or a project to design and implement a system over a three-month period (scheduled for 200 hours).

PROJECTS
Each group of students will carry out two projects on the following subjects:
Project 1 : 8 sessions
Study and implementation of a digital system on a FPGA ; example : video game like “pong” or “breakout”.
Project 2 : 6 sessions
Study and implementation of an application on a DSP or ARM core with a real-time operating system (RTOS).
Project 3: 4 sessions
Design of an analog ASIC with CADENCE EDA tools.

INDUSTRIAL STUDY OR PROJECT
Each group will carry out a project on an assembly defined by specifications established jointly with a manufacturer. The group will study the theoretical aspects, carry out the necessary experiments and produce the assembly. The subjects will be allocated during the first term and the project will take up an increasing proportion of the students’ time over the course of the second term. The students will be required to write detailed reports and to justify and present the work they have carried out. They will also give talks on their work so that their progress can be assessed.
List of the professors teaching in Major SERI

Véronique ALANOU Ingénieur ESEO, Professeur, campus de Rennes
Eric DENIAU Ingénieur Supélec, VP Engineering, ENENSYS, Rennes
Bruno DUFRIEN Ingénieur, responsable du labo de développement numérique, Thales Cholet
Dominique GUÉRIN Ingénieur Support outils CAD, S.A. ATMEL, Nantes
Yann Le Guillou Ingénieur Supélec, Docteur, RF platform lead architect, Renesas Mobile
Pierre LERAY Ingénieur INSA, Professeur, campus de Rennes
Dominique LEROUX Ingénieur ESME, Enseignant-chercheur à Télécom Bretagne, Brest
Yves LOUËT Ingénieur ISITV, Docteur de l’Université de Rennes I, Professeur, campus de Rennes
Didier LOUIS Ingénieur ECL et Supélec, Chef d’applications de Télécommunication, IBM France, Corbeil-Essonnes
Christian MOREAU Ingénieur INSA, Responsable du domaine d’expertise composants, DGA-MI, Bruz (35)
Christophe MOY Ingénieur INSA, Docteur INSA, Professeur, campus de Rennes
Amor NAFKHA Ingénieur SUP’COM Tunis, Docteur de l’Université de Bretagne Sud, Professeur, campus de Rennes
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