

ELECTRONIC SYSTEMS, NETWORKS and IMAGES

Professor in charge: Jacques WEISS

SERI

COURSES	CLASSES	EXAMS	SUBJECTS	ECTS Credits
15 h	6 h	1 WE	1 – ELECTRONICS Microelectronic Technologies	1
16,5 h	12 h	1 Exam	Hardware Architectures (FPGA & processors)	2
21 h	6 h	1 Exam	2 – ELECTRONIC SYSTEMS Digital SoC (Systems on Chip) design	2
15 h			Validation and Test of electronic systems	1
12 h	6 h	1 WE	3 – NETWORKS Digital Transmissions	2
12 h		1 Exam	Networks for Communication and Broadcast	1
13,5 h	3 h	1 Exam	4 – IMAGES Multimedia source coding and signal processing	2
6 h	6 h		Image Analysis and Synthesis	1
	18 half-days		5 – LAB WORK Three lab works	4
	50 half-days		Project or Industrial Study	8
			6 – Minores and foreign languages Six minors	12
			Seminar	2
			Foreign Languages	2
			7 - END OF STUDIES TRAINING PERIOD	20
	5 months april to september			
111 h	39 h 68 half-days lab works	6 exams		

WE: written exam

Exam : exam common with several courses (written or oral exam, or presentation)

The aim of the specialization in “Electronic Systems, Networks & Images” is to train highly skilled engineers in electronic systems, especially for nomad and mobile applications.

- *Signal processing with case studies for multimedia, digital communications and networks.*
- *Design of analog and digital electronics : define, in good adequacy between technology and applications, architecture of systems ; main performance targets are speed, cost, power consumption, integration density.*
- *Design management including methods and tools, necessary for engineers to specify, realize, test and qualify industrial products.*

A set of topical seminars on state of the art applications, delivered by industrialists, is used to illustrate the use of these techniques in the economic world.

The training is thus designed so as to allow the students to master methods and tools used in current developments, but also to be a driving force for future evolutions in a large industry spectrum.

Electronics

INTEGRATED ANALOG ELECTRONICS

15h C/ 6h BE / 1 exam / 2 ECTS credits

SERITM

Gilles Tourneur (7h30), Christian Moreau (7h30)

Different technological steps : processes and equipment

Obtaining the silicon. Thermal oxidation. Localised insulation. Epitaxy, diffusion, distribution and ion implantation. Photolithography. Polycrystalline and dielectric silicon deposition. Etching. Metal deposition.

Technology ways

Bipolar: description of the technology, implementation of NPN and PNP transistors, diodes, resistors and capacitors. MOS: NMOS, CMOS.

Faults, degradation mechanisms and technological improvements

Latch-up. Hot electron ageing. Oxides. Metal deposition.

Development of IC technology

Submicron CMOS. BICMOS. Gallium arsenide, silicon on insulator.

Production of integrated circuits

Development cycle for integrated circuits. Efficiency: line efficiency, electrical efficiency. Organisation of a FAB. Quality tools in the development cycle and production of integrated circuits: AMDEC/SPC /DOE/QFD.

Packaging and Interconnections

The packaging of electronic systems. Interconnections electronic components and integrated circuits. Thermal and electrical aspects of packaging. Reliability of micro-electronic assemblies. Interconnection processes and assembly methods. Electronic packaging evolution (roadmaps).

Bibliography :

M. MADOU, “Fundamentals of microfabrication”, CRC Press, 1997.

P. RAI-CHOUDHRY (Ed), “Handbook of Microlithography, micromachining and microfabrication”, SPIE Press, 1997.

HARDWARE ARCHITECTURES (FPGA and PROCESSORS)

16h30 C / 12h BE / 1 exam / 2 ECTS credits

SERIAM

Pierre Leray (6h), Jacques Weiss (9h), Renaud Séguier (1h30)

Microprocessors and associated components, which have been available since the first digital integrated circuits appeared in the early ‘70s, now form the core of most electronic products: they are found almost everywhere, particularly in information technology (from pocket calculators to computers), cars (ABS, injection systems, etc), automation equipment (programmable controllers, process control, etc) and domestic appliances (thermometers, remote controls, smart cards, etc).

Programmables devices (FPGA) (4,5 h C)

Programmable components can be used to implement extremely fast arithmetic logic functions in a short development time Due to technology improvements, it is now possible to integrate processor cores, this introduce the concept of SoPC (System On Programmable Chip).

The aim of this course is to place these programmable components in context with the other means of implementing a given task and to analyse the main architectures available on the market (Actel, Atmel, Altera, Xilinx, etc). After this analysis, student will be able to assess the enhancements provided by the new architectures and find the most suitable component for a given function.

Design approaches and market for programmable components

Criteria for selecting a particular technology: the technical, industrial and economic aspects.

Families of programmable components

From PAL and CPLDs, right through to FPGA: analysis of various architectures and their potential. Development of families and position in relation to the market.

Methodology and design tools

EDA tools.

Introduction to VHDL, description language for digital circuits and systems. Functional analysis and logic synthesis

Use of programmable components

Fields of application (signal processing, digital television, etc). Performance and limitations of the technology. Development systems.

Concept of SoPC (System on Programmable Chip)

Hard and Soft cores, reconfigurable hardware, dynamic reconfiguration

Microprocessors (12h C)

This course present the main architectural concepts used on state-of-the-art general purpose processors with analysis of the optimal adequacy with technology.

Structure and organisation of programmed systems

Central Unit

Memory : technologies and organisation.

Internal and external busses.

Peripheral components.

Processors architectures

RISC, CISC, VLIW and DSP architectures

Performance optimizations

 Hierarchy, technology and structure (cache insertion)

 Out-of-Order (speculative) sequencing

 Branch prediction

 Hyper-threading

Multiprocessing

Programming language (C langage)

Bibliography :

J.L. Hennessy, D.A. Patterson, "Computer Architecture, A Quantitative Approach", 3rd edition, M. Kaufmann, 2002.

W. Stallings, "Computer Organization and Architecture", 5th ed., 2000.

Structured Computer organisation, Prentice-Hall.

High performance reduced instruction set processors, IBM tech. Rep.

The cache memory book, Academic press.

Computer Architecture, Elsevier Science.

Bibliography :

J.L. Hennessy, D.A. Patterson, "Computer Architecture, A Quantitative Approach", 3rd edition, M. Kaufmann, 2002.

W. Stallings, "Computer Organization and Architecture", 5th ed., 2000.

Structured Computer organisation, Prentice-Hall.

High performance reduced instruction set processors, IBM tech. Rep.

The cache memory book, Academic press.

Computer Architecture, Elsevier Science.

Electronic Systems

DIGITAL SOC DESIGN

21h C / 6h BE / 1 examen / 2 crédits ECTS

SERICSI

Didier Louis (9h), Christophe Moy (3h), Amor Nafkha (3h), études de cas : Gérard Taroni (3h), Daniel Le Guennec (3h)

Les SoC (System on a Chip) résultent de l'augmentation de la puissance de traitement des équipements électroniques et des possibilités d'intégration offertes par la technologie ; ainsi, on regroupe sur une même puce un ou plusieurs processeurs, de la mémoire et de la logique hardware ; Il faut alors employer une méthodologie et des outils adaptés, de la conception jusqu'à la validation.

Introduction :

Electronic market technologies, prices and trends

Design techniques, description and comparison

ASIC technologies – Foundry/customer relationship

Design of circuits libraries

From base circuits up to complex functions (IP : Intellectual Property) – integrated memories self-test

Electrical and physical design.

System On a Chip

SOC core blocks

Processors cores – buses – reused logic.

The Reuse Methodology Manual.

SOC design

Specification – functional, architectural and hardware design

Systems design : platforms.

Memory design

DRAM - SRAM - non volatiles Memories.

Complex systems description and design, trends on design approaches

High-level Description Tools and languages, co-deign ; hardware/software partitioning ; heterogeneous platforms

Design of complex systems, trends of methods

High level digital flow of heterogeneous systems.

SystemC design flow .

Hardware-software partitioning. Cosimulation, modelisation

Abstraction levels (UTF, TF, TLM, RTL, ...).

Optimization and Operational research

Graphs theory. Scheduling. Resources allocation. Parallel computing

VALIDATION AND TEST OF ELECTRONIC SYSTEMS

15h C / 1 exam / 1 ECTS credit

SERIVTSE

Dominique Guérin (3h), Daniel Lambert (6h), Jacques Weiss (6h)

System testing is an important aspect of a manufacturer's strategy. It is used to measure the quality and reliability of products, and thus to validate the entire production sequence. The complexity and performance of systems are constantly increasing, so testing equipment is becoming ever more expensive. As a consequence, design strategies are needed that make testing easier, thus cutting costs. Testing must be carried out at every stage of production (from the integrated component and the printed circuit board, right through to the finished system). The testing equipment and strategies are therefore adapted to suit the particular context; characterization and maintenance also impose specific constraints.

Overview of the instrumentation used

Signal integrity, interconnections characterization, disturbance sources.

Power supply and parasitics rejection

Power supply circuits, specific components, decoupling.

Characterization

Functional verification,, static and dynamic characterization, functional and parametric tests. Fault diagnosis and location. Test bench: organisation and quantitative test flow.

Testing printed circuit boards

AOI (Automated Optical Inspection). In-Circuit test. Functional test. JTAG standard.

Testing integrated circuits

Testing with and without contact. Testing mixed circuits: analog and digital access.

Developments and trends

CAD and testing equipment. How far should the testing go? Development of new design and testing approaches.

Testability

Access limitations on integrated circuits, testability analysis, fault modelling and simulation ; test patterns generation (ATPG) ;
DFT : Design For Test.

NETWORKS

DIGITAL TRANSMISSIONS

12h C / 6h BE / 1 exam / 2 ECTS credits

SERITNM

Dominique Leroux (7,5h) , Yves Louët (4,5h).

Reliable data transmission in noisy environments requires the use of suitable methods. The aim of this course is to introduce the various digital modulation methods and their performance and to show how the combination of coding and modulation enables transmission performance to be enhanced.

Transmission channels

Wireless (Radio) channels modelling for indoor and outdoor communication. Wired, phone lines and power-line networks.

Digital modulation

Digital modulation principles. Various types of modulation: PAM, QAM, PSK, FSK

Digital demodulation

Principles and methods. Calculation of performance levels in the presence of noise.

Multi-carrier modulations

OFDM (DVB-T/H, ADSL) : Principles ; realization using an FFT operator.

Coded modulation : COFDM.

Spread-spectrum modulations

CDMA (UMTS, WiFi), choice criteria.

Carrier synchronization

Three case study practices :

- MAQ-16 modulations MAQ-16, error probabilities, comparison with MDP-2, effects of a bad synchronization.
- Simulation of a transmission chain ; study of adapted filters and Nyquist filters.
- OFDM application : DAB (Digital Audio Broadcasting).

Bibliography :

J.C. Bic, D. Duponteil, J.C. Imbeaux, "Éléments de communications numériques - Transmission sur fréquence porteuse", Collection technique et scientifique des télécommunications, CNET-ENST, Dunod, 1986.

J.G. Proakis, "Digital communications", McGraw-Hill International Editions, 1995.

M. Engels, "Wireless OFDM systems", Kluwer Academic Publishers, 2002.

N. Blaunstein, "Multipath phenomena in cellular networks", Artech House Books, 2003.

NETWORKS FOR COMMUNICATION AND BROADCAST

12h C / 1 exam / 1 ECTS credit

SERIRCD

Véronique Alanou (4,5h), Étienne Chevreau (3h), Eric Deniau (3h), Jacques Weiss (1,5h)

Any specialist in the field of architecture and integration of electronic systems is affected by data networks in two ways – first as the designer of components and equipment and second as a network user (CAD, production, etc). This course describes the architectural concepts of networks, public networks, local area networks and the available services ; media are also concerned such as radio and power-line networks.

Wide Area Networks (WAN)

The ATM (Asynchronous Transfer Mode) protocol : : physical layer, ATM layer, adaptation layer (AAL). ATM signalling – access control methods. LAN interconnection using ATM.

Frame Relay : signalling and admission control.

Multi Protocol Label Switching (MPLS) : notions on IP (Internet Protocol), Quality of Service (QoS), Virtual Private Network (VPN).

Protocols and networks SONET/SDH

Network characteristics, OSI reference model, QoS, nodal functions.

PDH/SDH protocols : PDH and SDH Hierarchies, SDH layers, SDH frames, QoS, protection mechanism, SONET/SDH standard

Wireless networks

IEEE 802.11 (WiFi) protocol

Power-Line networks

Introduction to Power-Line Communication, State of the art. Constraints and technical choices (example OFDM, Reed Solomon, Viterbi, filters).

Mobile phone networks (GSM, UMTS)

Network protocols and topology ; structure and frequency planning

Terrestrial Digital TV broadcast for nomad and mobile TV (TNT et DVB-H)

Broadcast networks protocols and topology ; structure and frequency planning

Bibliography :

H. Nussbaumer, "Téléinformatique", volumes 1 à 4, Presses Polytechniques Romandes.

G. Pujolle, "Les réseaux", Eyrolles

P. Rolin, "Réseaux hauts débits - Réseaux et télécommunications", Hermes.

A. Tanenbaum, "Réseaux", Prentice Hall - InterEditions.

A. Tanenbaum, "Réseaux : Architectures, protocoles, applications", InterEditions.

C. Servin, "Télécoms, de la transmission à l'architecture de réseaux", Collection Systèmes distribués.

Images

DIGITAL SIGNAL, SOUND AND IMAGE PROCESSING

13,5h C / 3h BE / 1 exam / 2 ECTS credits

SERICIS

Pierre Leray (7h30), Jacques Weiss (6h)

In addition to the filtering functions commonly encountered in processing systems, digital processing also allows the use of more powerful algorithms, such as adaptive filtering and prediction. These are used in speech compression operations, in particular. Real-time implementation of these algorithms requires the processing time to be taken into account and a compromise has to be made between performance and the number of calculations. The multi-rate structures are moving in this direction. Finally, the properties of the transforms (Fourier, cosine and wavelet transforms) also make analysis and processing much easier.

Digital processing

Signal digitization. Representation of numbers. Filtering functions (structures and synthesis).

Signal coding basis

Statistical signal properties, predictive and entropic coding (Huffman, Arithmetic, LZW, Golomb).

Adaptive filtering, linear prediction

Time and frequency-related algorithms. Speech processing applications.

Multi-rate processing systems

Structures. Filter banks. Sub-band coding.

Transforms (Fourier, DCT, wavelet)

Algorithms. Properties. Implementations.

Sound and image compression (MPEG)

Compression of the audio signal in radio communications and digital television (CELP, MUSICAM, Dolby AC3).

Image compression: transformation, quantization, motion estimation and compensation.

International standards : MPEG -1, -2 et -4/AVC, DCI (Digital Cinema)

Neural networks

Modelling the human brain. Structures. Learning algorithms.

3D image synthesis

3D models, vertex generation, texturing and fragment shading

Bibliography :

M. BELLANGER, "Traitement numérique du signal : théorie et pratique", Dunod.

V.K. MADISETTI, D.B.WILLIAMS, "The Digital Signal Processing Handbook", CRC Press.

P.P. VAIDYANATHAN, "Multirate Systems and Filter Bank", PTR Prentice Hall.

B. GOLD B, N. MORGAN, "Speech and Audio Signal Processing", Wiley.

S.J. SOLARI, "Digital Video and Audio Compression", McGRAW-HILL.

D.E. GOLDBERG, "Genetic Algorithms in Search, Optimization and Machine Learning", Ed. Addison-Wesley 1989.

F. I. PARKE, K. WATERS, "Computer Facial Animation", Ed. A K PETERS

IMAGE ANALYSIS AND SYNTHESIS

6h C / 6h BE / 1 exam / 1 ECTS credit

SERIASI

Renaud Séguier (6h)

The aim of this course is to present bases on 2D image analysis (filtering, segmentation) and on 3D image synthesis (meshes, texture rendering, morphing).

For pattern recognition, we present global methods and state-of-the-art tools and approaches.

Hardware implementation on generic or specialized platforms is studied

Image analysis (filtering, segmentation, pattern recognition)

3D image synthesis

Implementation (graphic accélérateurs , GPU, GPP, OpenGL)

Experimental work

Students will be divided into groups and will carry out laboratory work (long projects lasting 8, 6 and 4 sessions (half-days), for much of which they will be left to work on their own initiative and will be expected to set up, run and interpret the results of their experiments) and an industrial study or a project to design and implement a system over a three-month period (scheduled for 200 hours).

PROJECTS

Each group of students will carry out two projects on the following subjects:

Project 1: 8 sessions

Study and implementation of a digital system on a FPGA for data acquisition or signal processing (e.g. digital frequency demodulation, digital decimal filter, image compression).

Project 2 : 6 sessions

Study and implementation of a digital system using a DSP for data acquisition or signal processing (e.g. digital frequency demodulation, digital decimal filter, sound compression).

Project 3: 4 sessions

Design of an integrated circuit (e.g. coprocessor for digital filtering, FIFO memory using CMOS components, NICAM decoder, phase loop).

INDUSTRIAL STUDY OR PROJECT

Each group will carry out a project on an assembly defined by specifications established jointly with a manufacturer. The group will study the theoretical aspects, carry out the necessary experiments and produce the assembly. The subjects will be allocated during the first term and the project will take up an increasing proportion of the students' time over the course of the second term. The students will be required to write detailed reports and to justify and present the work they have carried out. They will also give talks on their work so that their progress can be assessed.

List of the professors teaching in Major SERI

Véronique ALANOU	Ingénieur ESEO, Professeur, campus de Rennes
Étienne CHEVREAU	Ingénieur Supélec, Technical Manager, SPIDCOM Technologies, Bourg-la-Reine
Eric DENIAU	Ingénieur Supélec, VP Engineering, ENENSYS, Rennes
Dominique GUÉRIN	Ingénieur Support outils CAD, S.A. ATMEL, Nantes
Daniel LAMBERT	Docteur de l'Université de Paris VI, Responsable Design physique des cartes électroniques, BULL, Les Clayes-sous-bois
Pierre LERAY	Ingénieur INSA, Professeur, campus de Rennes
Dominique LEROUX	Ingénieur ESME, Enseignant-chercheur à TÉLECOM Bretagne, Brest
Yves LOUËT	Ingénieur ISITV, Docteur de l'Université de Rennes I, Professeur, campus de Rennes
Didier LOUIS	Ingénieur ECL et Supélec, Chef d'applications de Télécommunication, IBM France, Corbeil-Essonnes
Christian MOREAU	Ingénieur INSA, Responsable du domaine d'expertise composants, CELAR, Bruz (35)
Christophe MOY	Ingénieur INSA, Docteur INSA, Professeur, campus de Rennes
Amor NAFKHA	Ingénieur SUP'COM Tunis, Docteur de l'Université de Bretagne Sud, Professeur, campus de Rennes
Renaud SÉGUIER	Docteur de l'Université de Rennes I, Professeur, campus de Rennes
Gérard TARONI	Ingénieur ISEP, Responsable conception ASICs, IBM France, Corbeil Essonnes
Gilles TOURNEUR	Ingénieur Supélec, Docteur de l'Université de Rennes I, Professeur, campus de Rennes
Jacques WEISS	Ingénieur Supélec, Docteur de l'Université de Rennes I, Professeur, campus de Rennes