
Filtering Lab

Background

Altera provides DSP MegaCore® functions that perform signal generation and filtering. This lab uses an example design that implements the NCO compiler for signal generation and the FIR compiler for filtering. The lab also uses a PC application, which lets you view the unfiltered and filtered signals without an oscilloscope.

The example design generates two sinusoids and executes a 3-MHz low-pass fixed FIR filter. Data is transferred to the Windows application in blocks of 1k words. The design has the following elements:

- 40-MHz input clock
- NCO compiler for signal generation
- FIR compiler for filtering
- Nios embedded processor to control the PC interface via RS-232 port and to perform data buffering
- Analog to digital (A/D) and digital to analog (D/A) capture control circuitry

The design files are installed when you install the software on the *APEX DSP Development Kit CD-ROM*. You can view the top-level schematic in the Quartus II software. This lab consists of the following exercises:

- *Exercise 1*—In this exercise you will review the filtering design using the Quartus® II software.
- *Exercise 2*—In this exercise you will configure the APEX™ device with the filtering design and use a Windows application to view filtered and unfiltered data.
- *Exercise 3*—In this exercise you will use the MATLAB and Simulink software to view the Altera-generated models of the filtering design.

Before You Begin

These instructions assume that you have already installed the software provided with the APEX DSP Development Kit onto your PC. If you have not done so, refer to the *APEX DSP Development Kit Getting Started User Guide* for installation instructions. You must also have the following software installed on your PC:

- Quartus II version 1.1 (limited edition or a purchased version)
- MATLAB version 6.0 or higher
- Simulink version 4.0 or higher




This white paper assumes that you have installed the software into the default locations.

Before performing the exercises, you must connect cables to the AEPX DSP board. Refer to the *APEX DSP Development Kit Getting Started User Guide* for detailed instructions on how to connect the cables to the board. Perform the following steps to connect the cables:

1. Connect the power adapter cable to the board and plug it into a power outlet.
2. Connect the SMA cable to D/A 1 and A/D 1 on the board.
3. Connect the RS-232 cable to your PC and to the board.

Exercise 1: Review the Filtering Design

Review the filtering design by perform the following steps:


1. Run the Quartus II software.
 2. Choose **Open Project** (File menu).
 3. Browse to the directory `c:\MegaCore\dsp_development_kit-v1.0.0\labs\filtering\quartus`.
 4. Select the project `all_on_chip_32.quartus`. Click **OK** if you receive an overwrite warning message.
 5. Click **Open**. The schematic file `all_on_chip_32.bdf` opens.
 6. Add the FIR compiler and NCO compiler user libraries to the project.
 - a. Choose **General Settings** (Project menu).
 - b. Click the **User Libraries** tab.
 - c. Click **Add**.
 - d. Browse to the directory in which the FIR compiler was installed. The default installation directory is `c:\MegaCore\fir_compiler-v2.3.1\lib`.
 - e. Click **Open**.
 - f. Repeat steps **a** through **e** for the NCO compiler. The default installation directory is `c:\MegaCore\nco-v1.3.0\lib`.
 7. Choose **Save As** (File menu).
 8. Click **Save**.
 9. A message appears that the file already exists and you are asked if you want to replace it. Click **Yes**.
 10. Review the schematic design.
 - a. Double-click the `filt_lp` block, which is the FIR compiler block, to view the parameters that were specified in the wizard. Designing a typical FIR filter in hardware can take up to 6 weeks. Using the FIR compiler, this filter was created in a day. This filter design only requires 40-MHz filter performance; however, the FIR compiler can achieve performance over 200 MHz. Click **Cancel** to close the wizard.
 - b. Double-click the `NCO` block, which is the NCO compiler block, to view the parameters that were specified in the wizard. This design uses a small-ROM implementation, which only requires 45 degrees of storage to create a spectrally pure sinusoid. The NCO compiler lets you make architecture trade-offs to use the fewest device resources while meeting your specific design requirements. This ROM-based implementation operates at 40-MHz; however, the NCO compiler can achieve performance up to 200 MHz. Click **Cancel**.
 - c. Perform the same action on the `PLL` block to view its setting. Click **Cancel** to close the wizard.
-  The filtering design implements a Nios embedded processor to control the RS-232 data flow and to perform data buffering. However, the Nios embedded processor is not provided in the APEX DSP Development Kit. You must purchase a license for the Nios processor if you want to recompile the design.
11. Choose **Close Project** (File menu) when you are done reviewing the file.

Exercise 2: Generate Signals & Filter

In this exercise you will configure the APEX device on the APEX DSP development board with the filtering design and then use a Windows application to view unfiltered and filtered data. The 2 NCOs generate 2 sinusoids, which are added together and converted from digital to analog via the on-board D/A converters. The signal exits the board via the D/A SMA connector, loops back into the board through the A/D SMA connector, and is converted to digital by the on-board A/D converters, and re-enters the APEX device. (If the loop back does not occur, you will not see a signal in the application.) The signal is then filtered if this option is selected in the application. The design has been compiled with a 3-MHz low-pass filter.

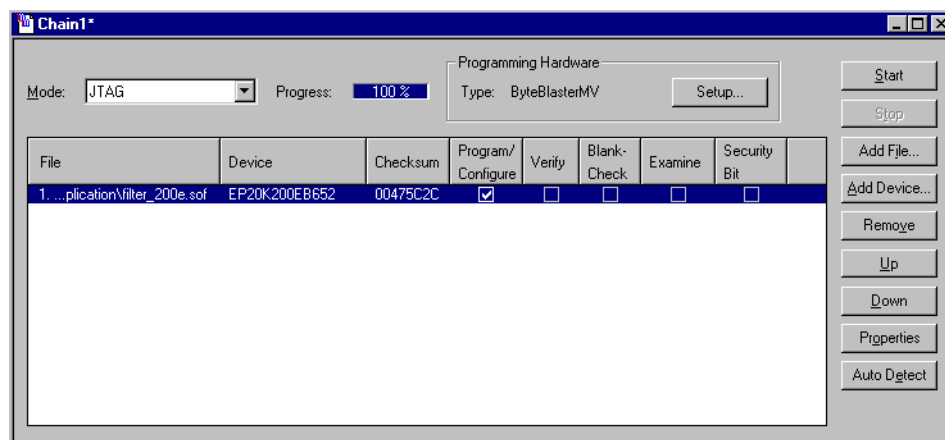
Configure the APEX Device


Perform the following steps to configure the device.

 The board ships pre-programmed with the filtering design described in this lab. You only need to perform these steps if you have reprogrammed the EPC16 device on the board.

1. Choose **Programs > Altera > Quartus II 1.1 Limited Edition** (Windows Start Menu).
2. Choose **Open Programmer** (Processing menu).
3. Click **Add File**.
4. Browse to the **c:\MegaCore\dsp_development_kit-v1.0.0\labs\filtering\application** directory.
5. If you are using the starter version of the APEX DSP development board, select the **filter_200e.sof** file; for the professional version, select the **filter_1500e.sof** file.
6. Click **Open**.
7. Turn on the **Program/Configure** option.
8. Click **Start** to configure the APEX device. [Figure 1](#) shows the Programmer after the APEX device is configured.

Figure 1. Quartus II Programmer



 When you close the Programmer, you may be asked if you want to save Chain1. Click **No**.

Run the Windows Application

The windows application displays the results of the filtering design. Figure 2 describes the application options.

Figure 2. Windows Application Options

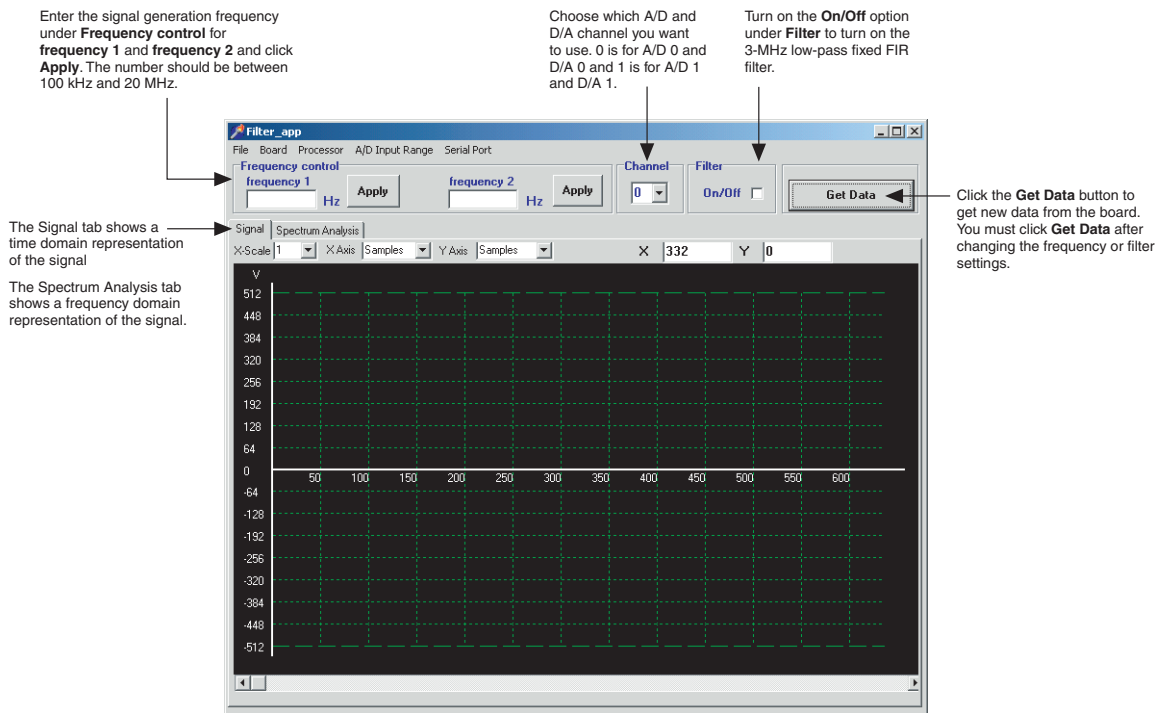


Table 1 describes the application menu options.

Table 1. Windows Application Menu Commands

Menu	Command	Function
File	Save Signal	Select this command to save the signal data as a text file. You can then plot the signal in other graphing tools.
	Save Spectrum	Select this command to save the spectrum data as a text file. You can then plot the spectrum in other graphing tools.
Board	1500E	Select this option is you are using the professional board.
	200E	Default option. Select this option is you are using the starter board.
Processor	Load Nios	Loads a program into the Nios embedded processor.
A/D Input Range	+/- 0.5 Volt	Default option. This option should match the A/D configuration on the board. Refer to the A/D section of the APEX DSP board data sheets for information on configuring the board.
	+/- 1 Volt	This option should match the A/D configuration on the board. Refer to the A/D section of the APEX DSP board data sheets for information on configuring the board.
Serial Port	COM1, COM2, COM3, COM4	Indicate which port the serial cable is connected to on your PC.

To run the Windows application, perform the following steps:

1. Choose **Run** (Windows Start menu).
2. Click **Browse**.


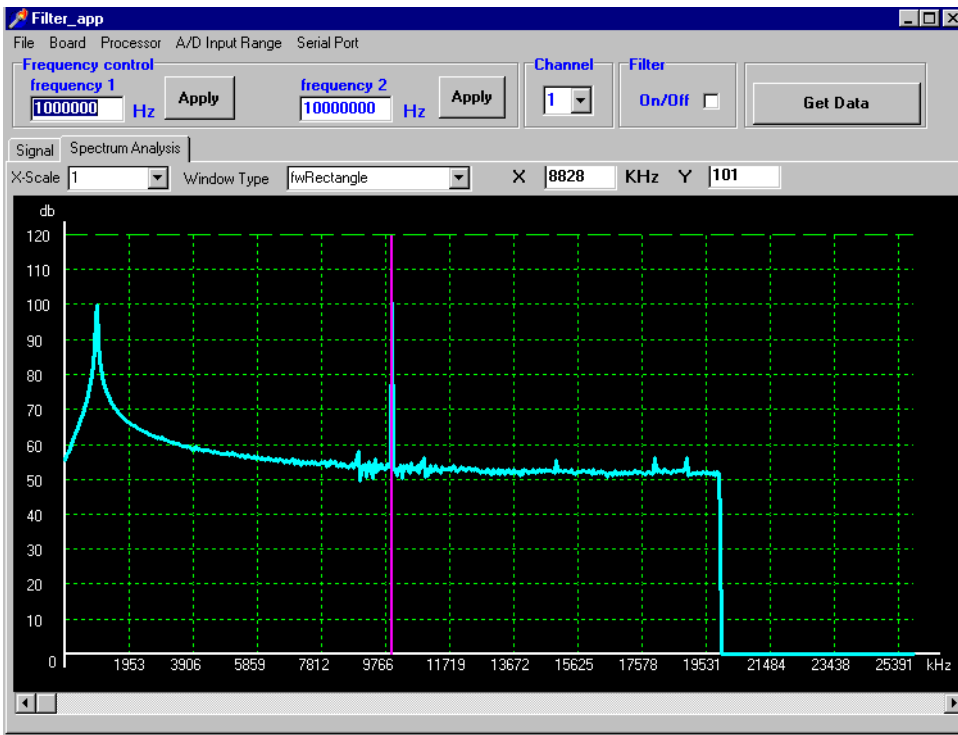
3. Browse to the `c:\MegaCore\dsp_development_kit-v1.0\labs\filtering\application` directory.
4. Select the file **Filter_App.exe**.
5. Click **Open**.
6. Click **OK**. The **Filter_app** window opens.
7. If you connected the RS-232 cable to a port other than COM 1, choose the port in the Serial Port menu.
8. Choose **Load Nios** (Processor menu).
9. Select the file **disp.srec**.
10. Click **Open**. The program is loaded into the Nios embedded processor on the board.
11. If you are using the professional board, choose **1500E** (Board menu). If you are using the starter board, the **200E** option, which enables the starter board, is turned on by default.
 If you are using the starter board and **200E** is selected in the Board menu, do not select it again. If you do so, the application selects the **1500E** instead.
12. Enter 1000000 (6 zeros) in the **frequency 1** box and click **Apply** to set the NCO 1 frequency.
13. Enter 10000000 (7 zeros) in the **frequency 2** box and click **Apply** to set the NCO 2 frequency. Leave all other settings as is.
14. Click **Get Data**. The NCO frequencies 1 and 2 are added together.
15. The display in the **Signal** tab, which is selected by default, shows the unfiltered data in time (see [Figure 3](#)). Click the **Spectrum Analysis** tab to view the frequency domain (see [Figure 4](#)).
16. Click in the display to enable a vertical line cursor. You can use the right and left arrow keys to move the cursor right or left, respectively.

Figure 3. Unfiltered Signals in the Time Domain



Figure 4. Unfiltered Signals in the Frequency Domain



17. Turn on the **On/Off** option under **Filter**. The filter is a 3-MHz, low-pass filter. Therefore, the filter should remove the 10-MHz sinusoid.
18. Click **Get Data** to view the results. See [Figures 5](#) and [6](#).

Figure 5. Filtered Signal in Time Domain

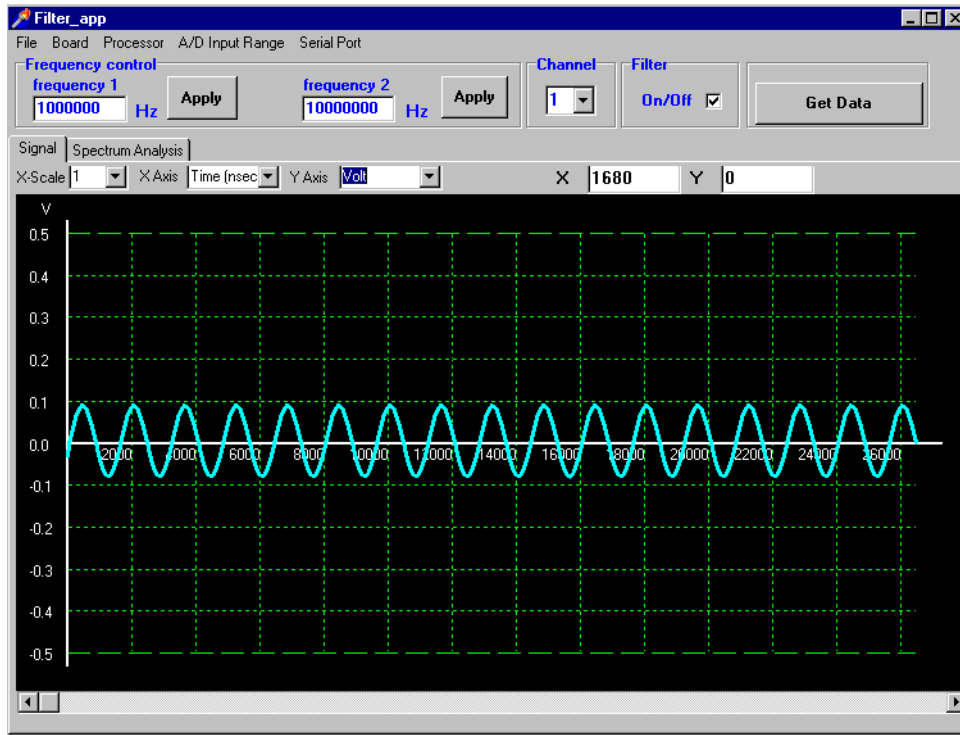
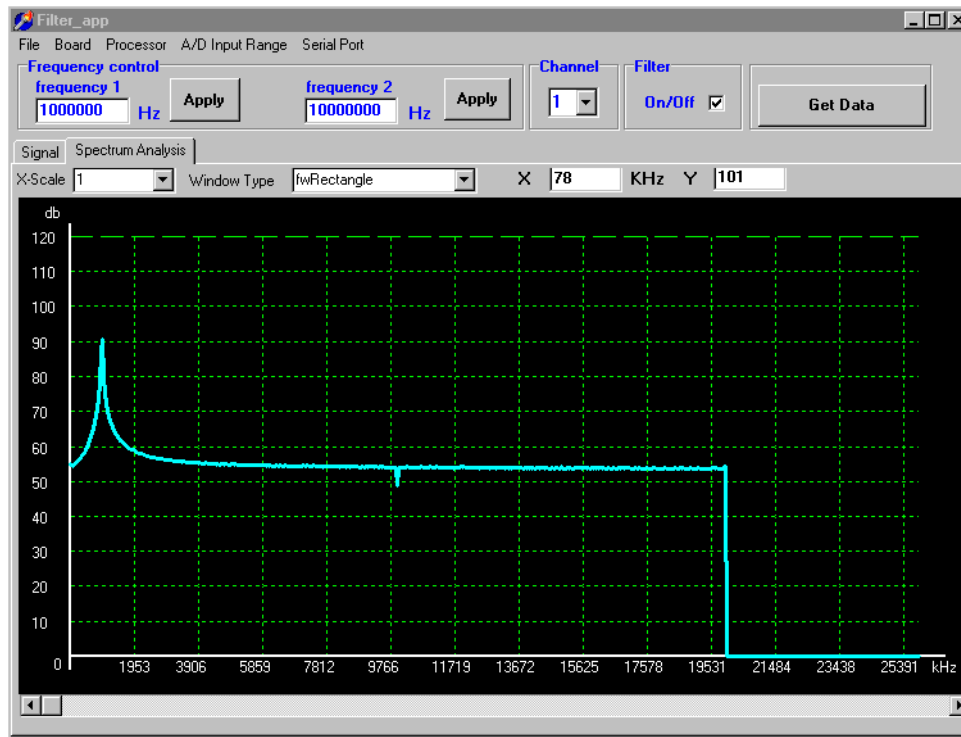



Figure 6. Filtered Signal in Frequency Domain



You can specify other frequencies for the NCO under **Frequency control** to view the operation of the filtering application with different frequencies (between 100 kHz and 20 MHz).

Exercise 3: Analyze the Design in MATLAB & Simulink

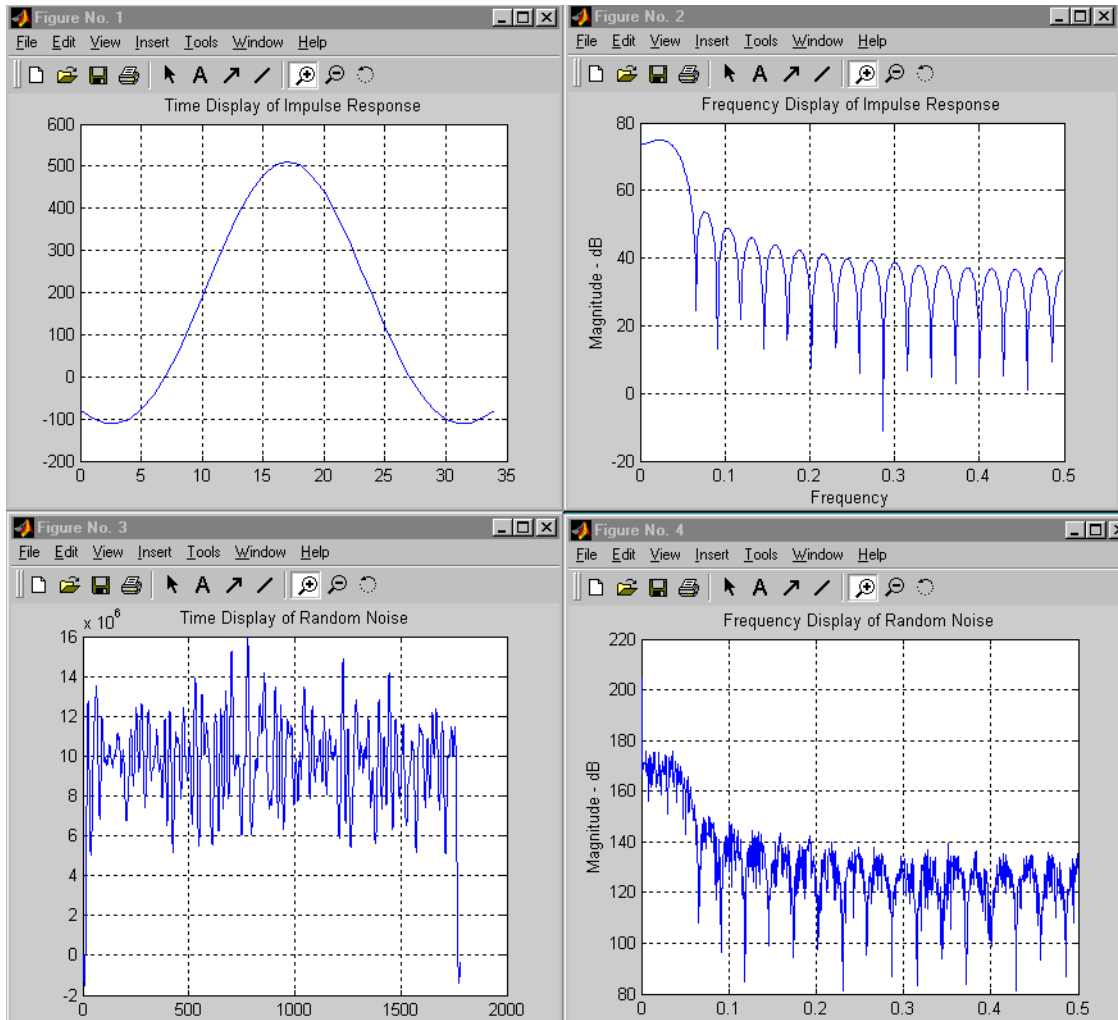
The Altera FIR compiler and NCO compiler wizards can generate MATLAB M-Files and Simulink models. In this exercise, you will use these files to analyze and simulate the design.

 These instructions assume that you are familiar with the MATLAB and Simulink software. Refer to the on-line help for these software products for information on how to use them.

MATLAB Filter Analysis

1. Run the MATLAB software.
2. Set your current directory to `c:\MegaCore\dsp_development_kit-v1.0.0\labs\filtering\quartus`.
3. Type the command `filt_lp_qplot` in the **Command Window**. Four figure windows display (stacked on top of each other). Move the windows to view the results. See [Figure 7](#).

Figure 7. MATLAB View



Simulink Simulation

Perform the following steps to create a model in Simulink and simulate.

1. Choose **New > Model** (File menu) in the MATLAB software.
2. Choose **Open** (File menu) in the new model window.
3. Select the **nco.mdl** file and click **Open**.
4. Drag and drop the Altera NCO block into the new design.
5. Close the **nco.mdl** file.
6. Choose **Open** (File menu) in the new model window.
7. Select the **fir_lp_parallel.mdl** file and click **Open**.
8. Drag and drop the Altera FIR Filter block into the new design.

9. Close the `fir_lp_parallel.mdl` file.
10. Open the Simulink Library Browser.
11. Drag and drop a Constant block from the Sources library into your model and place it to the left of the Altera NCO block.
12. Draw a connection line from the Constant block to the `phi_inc_j` port on the Altera NCO block.
13. Copy the Constant block and Altera NCO block and paste it below the one in the model file. The new blocks are automatically named Contant1 and Altera NCO1.
14. Double-click on the Constant block.
15. Enter 107374182 in the Constant value box and click **OK**.
16. Double-click on the Constant1 block.
17. Enter 1073741824 in the Constant value box and click **OK**.


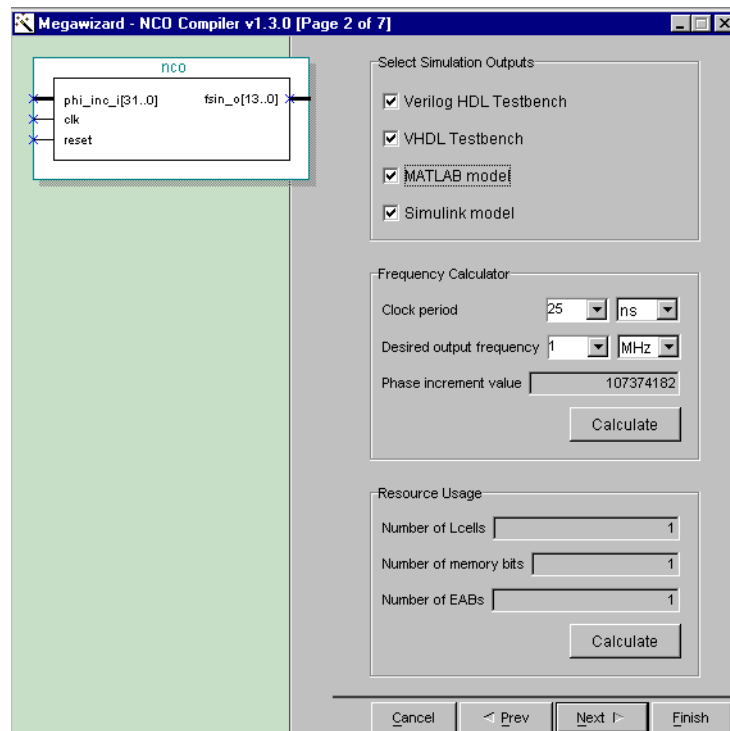
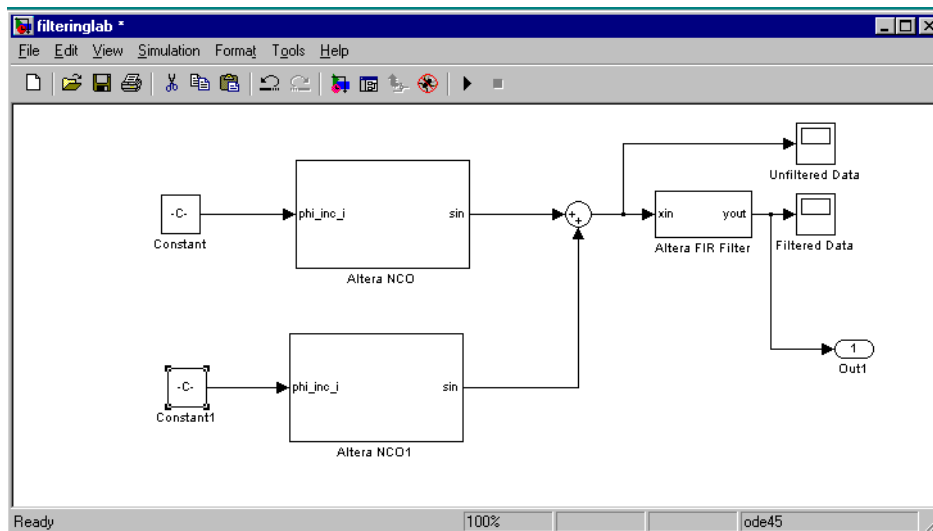
 The constants determine the frequency of the NCO sine outputs. The NCO wizard calculates the constant when you enter the clock period and the desired output frequency in the wizard. [Figure 8](#) shows the calculated result for a 1 MHz sine wave (107374182). The chosen clock period corresponds to the 25 ns (40 MHz) oscillator on the APEX DSP development board. Similarly, the desired output frequency of 10 MHz yields a phase increment value of 1073741824.

Figure 8. Calculating Phase Increment Value in the NCO Wizard



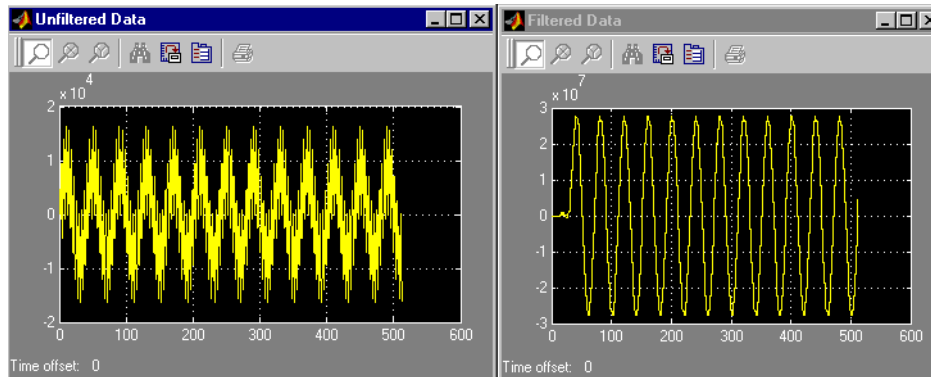
18. Drag and drop a Sum block from the Math library into your model and position it to the right of the Altera NCO block. This block adds the results of the sinusoids generated by the NCOs. Draw connection lines from the `sin` ports of the two NCO blocks to the Sum block.
19. Draw a connection line from the Sum block to the `xin` port on the Altera FIR Filter block
20. Drag and drop two Scope blocks from the Sinks library into your model, positioning them above and to the right of the Altera FIR Filter block.
21. Draw a connection line from one Scope to the line between the Sum block and the Altera FIR Filter block. This scope will show the unfiltered data.
22. Draw a connection line from the Altera FIR filter block to the second Scope block. This scope will show the filtered data.
23. Drag and drop the Out1 block from the Signals & Systems library (MATLAB version 6.0) or Sinks library (version 6.1) into the model and position it below and to the right of the Altera FIR Filter block. This block allows the Simulink output to be placed in the MATLAB work space so that an FFT plot of the output can be generated.
24. Draw a connection line from the Out1 block to the line between the Altera FIR Filter block and the filtered data scope. [Figure 9](#) shows the completed model.

Figure 9. Simulink Model



25. Choose **Simulation Parameters** (Simulation menu).
26. Enter 1048.0 in the **Stop time** box.
27. Click **OK**.
28. Choose **Start** (Simulation menu) to run the simulation.
29. When simulation completes, double-click on the scopes to view unfiltered data and filtered signals in time domain. Click the binoculars icon to auto-scale the scopes. See [Figure 10](#).

Figure 10. Signals in Time Domain



30. Switch to the MATLAB window. You will now view the FFT of the filtered output using the `fftnlplot` file, which is included with the lab.

31. Type the following command in the MATLAB Command Window:

```
fftnlplot(yout, 'Frequency Response', 4e7, 'r')
```

where:

`yout` is the name of the signal represented by Out1 in the Simulink model.

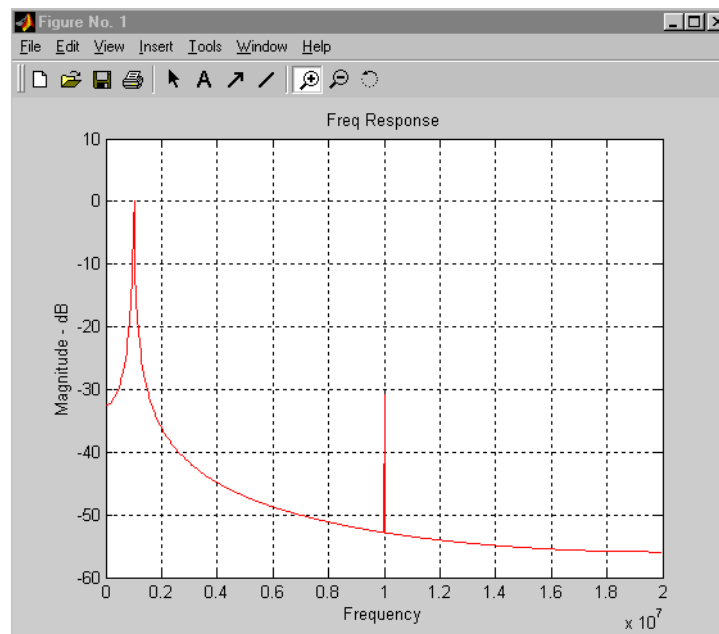
Frequency Response is the title of the plot.

`4e7` is the sampling frequency (40 MHz).

`r` is the color of the plot line.

Figure 11 shows the plot, which is the frequency response of the filter output.

Figure 11. FFT Response





101 Innovation Drive
San Jose, CA 95134
(408) 544-7000
<http://www.altera.com>

Copyright © 2001 Altera Corporation. Altera, The Programmable Solutions Company, the stylized Altera logo, specific device designations, and all other words and logos that are identified as trademarks and/or service marks are, unless noted otherwise, the trademarks and service marks of Altera Corporation in the U.S. and other countries. All other product or service names are the property of their respective holders. Altera products are protected under numerous U.S. and foreign patents and pending applications, maskwork rights, and copyrights. Altera warrants performance of its semiconductor products to current specifications in accordance with Altera's standard warranty, but reserves the right to make changes to any products and services at any time without notice. Altera assumes no responsibility or liability arising out of the application or use of any information, product, or service described herein except as expressly agreed to in writing by Altera Corporation. Altera customers are advised to obtain the latest version of device specifications before relying on any published information and before placing orders for products or services. All rights reserved.