White Paper

DSSS Modem Lab

Background

The direct sequence spread spectrum (DSSS) digital modem reference design is a hardware design that has been optimized for the Altera® APEX™ DSP development board (starter version), which features an APEX EP20K200E device. The reference design is a spread spectrum modulator/demodulator subsystem that can be used as a starting point for a complete 3G or fixed wireless modem. The design highlights the ease of use, performance, and efficiency of implementing a design using Altera devices and DSP intellectual property (IP) cores.

The design uses the correlator, FIR compiler, and NCO compiler MegaCore® functions, and uses 7,183 logic cells and achieves 100-MHz performance. A parameterizable UART and a Windows application enables communication between the APEX DSP development board and a PC via the board's RS-232 interface, yielding a true development platform for intermediate frequency (IF) modem designs. The reference design includes VHDL source code (except for the IP cores), and a simulation library and test bench for simulation in ModelSim simulators.

Altera provides a Windows application that graphically displays the input and resulting output data from the modem. Using the application, you can examine the effects of random channel phase and the demodulator's ability to re-synchronize itself. You can also investigate the effects of using non-identical spreading codes or complex codes with poor orthogonality. For technical specifications of the reference design and a brief overview of spread spectrum communications, refer to *FS 14: Direct Sequence Spread Spectrum (DSSS) Modem Reference Design*.

In this lab you will use an Altera-provided SRAM Object File (**.sof**) for the pre-compiled DSSS modem reference design to confirm the valid operation of the modem. The design files and Windows application are installed when you install the software on the ***APEX DSP Development Kit CD-ROM***. This lab includes the following exercises:

- *Exercise 1*—In this exercise you will review the DSSS modem design using the Quartus® II software.
- *Exercise 2*—In this exercise you will configure the APEX device with the DSSS modem design.
- *Exercise 3*—In this exercise you will use a Windows application to view a graphical display of the input and resulting output data from the modem.

Before You Begin

These instructions assume that you have already installed the software provided with the APEX DSP development kit onto your PC. If you have not done so, refer to the ***APEX DSP Development Kit Getting Started User Guide*** for installation instructions. You must also have the following software installed on your PC:

- Quartus II version 1.1 (limited edition or a purchased version)

☞ This white paper assumes that you have installed the software into the default locations.

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Before performing the exercises, you must connect cables to the AEPX DSP board. Refer to the ***APEX DSP Development Kit Getting Started User Guide*** for detailed instructions on how to connect the cables to the board. Perform the following steps to connect the cables:

1. Connect the power adapter cable to the board and plug it into a power outlet.
2. Connect the ByteBlasterMV cable to your PC and to the board's 10-pin JTAG header for APEX configuration.
3. Connect the RS-232 cable to your PC and to the board.

Exercise 1: Review the DSSS Modem Design

Review the filtering design by perform the following steps:

1. Run the Quartus II software.
2. Choose **Open Project** (File menu).
3. Browse to the directory **c:\MegaCore\dsp_development_kit-v1.0.0\reference_design\dsss\quartu**s.
4. Select the project file **top_level_dsss.quartus**.
5. Click **Open**. The schematic file **top_level_dsss.bdf** opens.
6. Add the FIR compiler and NCO compiler user libraries to the project.
   a. Choose **General Settings** (Project menu).
   b. Click the **User Libraries** tab.
   c. Click **Add**.
   d. Browse to the directory in which the FIR compiler was installed. The default installation directory is **c:\MegaCore\fir_compiler-v2.3.1\lib.**
   e. Click **Open**.
   f. Repeat steps a through e for the NCO compiler. The default installation directory is **c:\MegaCore\nco-v1.3.0\lib**.
7. Choose **Save As** (File menu).
8. Click **Save**.
9. A message appears that the file already exists and you are asked if you want to replace it. Click **Yes**.
10. Review the schematic design. You can view the reference design as a schematic by browsing the hierarchy tree in the Quartus II Project Navigator and clicking on the sub-level designs. The top-level design file, **top_level_dsss.bdf** instantiates the DSSS modem, PLL,UART, and UART interface.
    a. Browse to the right side of the schematic to the DSSS modem symbol.
    b. Right-click the symbol and choose **Open Selected Entity**. The modem schematic, **dsss.bdf**, opens in a new window.

The modem design file instantiates the pilot sequence generator, the modulator, the channel model, and the demodulator. The pilot generator generates the pilot channel data; the modem receives the data channel from the Windows application via the UART interface.

c. Right-click the modulator symbol and choose **Open Selected Entity**. The modulator schematic, named **modulator.bdf**, opens in a new window.

d. Scroll the **modulator.bdf** window from left to right to view the modulator design entities. The design contains a combination of MegaCore functions, library of parameterized modules (LPM) functions, and custom logic. The 2-channel interpolating FIR filter is to the right of the complex spreader and FSM.

e. Double-click the FIR filter symbol to launch the FIR compiler wizard. The FIR compiler wizard can generate a variety of filters, including this 67-tap root-raised cosine filter with an excess bandwidth of 22%. This design uses a serial, polyphase-decomposed interpolating filter with a cut-off frequency of 4 MHz.

f. Click **Cancel** to close the FIR compiler wizard.

g. The up-converting mixer follows the buffering FIFO symbols. Double-click the `nco_mod` symbol to launch the NCO compiler wizard. The design uses a small ROM implementation and an output precision of 12 bits from a 24-bit phase accumulator. The quadrature outputs from the NCO are modulated with the output of the pulse-shaping filter using multipliers and added to form the digital IF signal. Both arithmetic functions were implemented using multiplier and adder LPM functions. The IF output passes to the channel model.

h. Click **Cancel** to close the NCO compiler wizard.

i. Close the **modulator.bdf** window and return to the DSSS modem schematic **dsss.bdf**.

   The channel model follows the modulator and uses the IF signal from the modulator as input. The channel also uses a signal channel select as an input. This input is tied to push-button switch SW2 on the APEX DSP development board and introduces random data as input to the demodulator when you press the switch. The output from the channel is passed to the demodulator.

j. Right-click the demodulator symbol and choose **Open Selected Entity**. The demodulator schematic opens in a new window named **demodulator.bdf**.

k. Scroll the **demodulator.bdf** window from left to right to view the demodulator design entities. The input signal passes through an initial symbol recovery circuit before being down-converted by multipliers and a demodulating NCO, identical to the modulator NCO. The resulting output is filtered by two FIR filters. Following down-conversion, the signals are decimated being despread by the oversampling complex-mode correlator, which was designed using the correlator MegaCore function, and a peak-detection circuit. The synchronization block below the correlator monitors the despread pilot channel output of the peak-detection circuit and feeds control information back to the symbol recovery block at the beginning of the demodulator. It also outputs a lock signal, indicating whether the receiver has acquired synchronization.

l. Close the **demodulator.bdf** window and the DSSS modem schematic **dsss.bdf**.

m. In the top-level design schematic, **top_level_dsss.bdf**, observe the modem output. It outputs a synchronization lock signal (from the synchronization monitor), which sent to LED D6 on the APEX DSP development board. When the LED is off, the demodulator is synchronized to the modulator. The modem also outputs the despread data channel and passes it back to the UART interface where it is transmitted to the PC for viewing in the waveform viewer application.

11. Choose **Close Project** (File menu) when you are done reviewing the file.

Exercise 2: Configure the APEX Device

Perform the following steps to configure the device:

1. Choose **Programs > Altera > Quartus II 1.1 Limited Edition** (Windows Start Menu) or **Programs > Altera > Quartus II 1.1** (Windows Start Menu).

2. Choose **Open Programmer** (Processing menu).

3. Click **Add File**.

4. Browse to the **c:\MegaCore\dsp_development_kit-v1.0.0\reference_design\dsss\quartus** directory.

5. Select the file **top_level_dsss200E.sof** if you are using the APEX DSP development board starter version; select the file **top_level_dsss1500E.sof** if you are using the professional version.

6. Click **Open**.

7. Turn on the **Program/Configure** option.

8. Click **Start** to configure the APEX device.

Exercise 3. Run the Windows Application

The windows application displays the results of the filtering design.

Run the Windows Application

To run the Windows application, perform the following steps:

1. Choose **Run** (Windows Start menu).

2. Click **Browse**.

3. Browse to the **c:\MegaCore\dsp_development_kit-v1.0.0\reference_design\dsss\application** directory.

4. Select the file **dsss.exe**.

5. Click **Open**.

6. Click **OK**. The **Altera DSSS Reference Design** window opens.

Enter Modem & Waveform Viewer Initialization Data & Parameters

To initialize the DSSS modem reference design and parameterize the waveform viewer, perform the following steps:

1. Select the PC serial port through which you want to communicate to the APEX DSP development board under **PC Port Selection** in the application.

2. Type the name of the input source file you want to download as binary data input to the modem in the **Input Data File** box under **Input File**.

   ☞ Altera provides two source data files with the reference design, which you can use as the input source file. The file **count.txt** contains data forms a modulo-8 counter and the file **uniform.txt** is a repeating 8-bit sequence. These data streams have been chosen to illustrate the operation of the modem in the event of channel phase shifts and/or unmatched spreading codes. However, you can also use your own data file. The application reads data from the file as a long binary string (2,048 bits) before outputting it to the serial port. Therefore, your input file should contain a binary string without newline characters.

3. Select the length-16 spreading and despreading codes you wish to use in the modulator and demodulator for the data channel component of the channelization codes under **Channelization Code Selection**. (The pilot channel component of the complex spreading codes is fixed on both sides of the channel. Its channelization code is set as `1010101010101010`.) For correct operation, the **Despreading Code** and **Spreading Code** selections must be identical. However, you can experiment with different codes to monitor the effects of using non-identical codes.

4. Select the duration for which you want to plot the input and output data streams in the **Plot results for** box under **Run-Length**. The modem operates continuously and does not stop after this interval. However, due to the high data rates of the input and corresponding output sequences only portions of the data are displayed in the application waveform viewer at a time. Selecting a given time interval (<500 seconds) allows you to reset the device and re-run the application with a new set of channelization codes and/or input data sequences.

5. Reset the APEX device by pressing the push-button switch SW0 (the master reset) on the APEX DSP development board. The SW0 switch is tied to the APEX device `DEVCLRn` pin. Therefore, your should press down on the switch for at least 3 seconds to that the design operates properly.

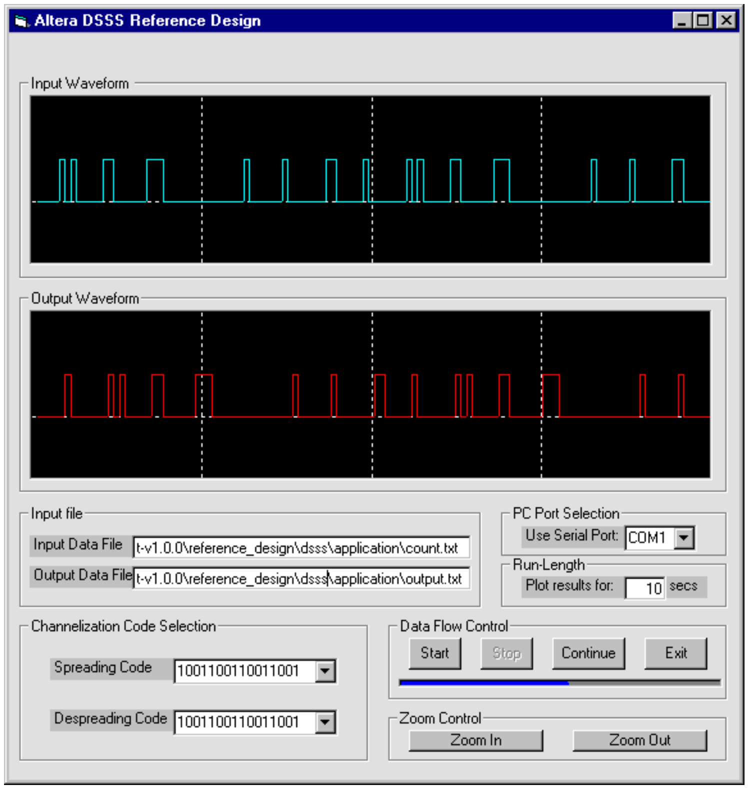
Start the DSSS Modem Operation

When you finish setting the parameters and initialization data, perform the following steps to start the modem.

1. Click **Start** under **Data Flow Control**. The selected codes and input binary stream are downloaded to internal memory in the APEX 20KE device via the RS-232 port. The waveform viewer displays the modem input and resulting output waveforms. You can use the **Zoom In** and **Zoom Out** buttons under **Zoom Control** to adjust the window size over which data is plotted. See Figure 1.

☞ You can stop the waveform viewer at any time by clicking **Stop** under **Data Flow Control**. To continue viewing the results, click **Continue**. Click **Exit** to close the application.

Figure 1. DSSS Reference Design Windows Application



2. Press the push-button switch SW2 on the APEX DSP development board, holding it down for a short period of time. While the switch is pressed, the channel passes random data to the demodulator—forcing it to lose synchronization—and the output no longer matches the input. When you release the switch, the modulated data is passed to the receiver again.

   You can observe synchronization lock by watching LED D6 on the board. When the receiver loses lock, LED D6 turns on. When the modulator reacquires synchronization the LED turns off.

To operate the modem with new channelization codes and input data sequences, you **must** reset the modem by pressing SW0 on the APEX DSP development board before clicking **Start** again.

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