

Features

- Powerful development board for digital signal processing (DSP) designs featuring the APEX™ EP20K200E-1X device in a 652-pin package (ordering code: DSP-BOARD/A2E)
- Analog I/O
 - 2 10-bit 40-MHz A/D converters
 - 2 10-bit 125-MHz D/A converters
 - Active filtering of analog inputs and outputs
 - Single-ended analog I/O
- Digital I/O
 - 3.3-V expansion/prototype headers over 200 user I/O pins
 - RS-232 serial port
- Memory subsystem with 256 Kbytes of 12-ns asynchronous SRAM
- Configuration options
 - On-board configuration via the 16 Mbit EPC16 flash configuration device
 - Download configuration data using ByteBlasterMV™ download cables
- Debugging port with a 3.3-V logic analyzer (four 8-bit headers with ground pins)
- Additional features:
 - Four user-definable slide switches
 - Three user-definable push-button switches
 - Three user-definable LEDs
 - Prototyping area
 - On-board oscillator
 - External oscillator input
 - Seamless assembly of multi-board systems
- Single 5-V DC power supply (adapter included)

General Description

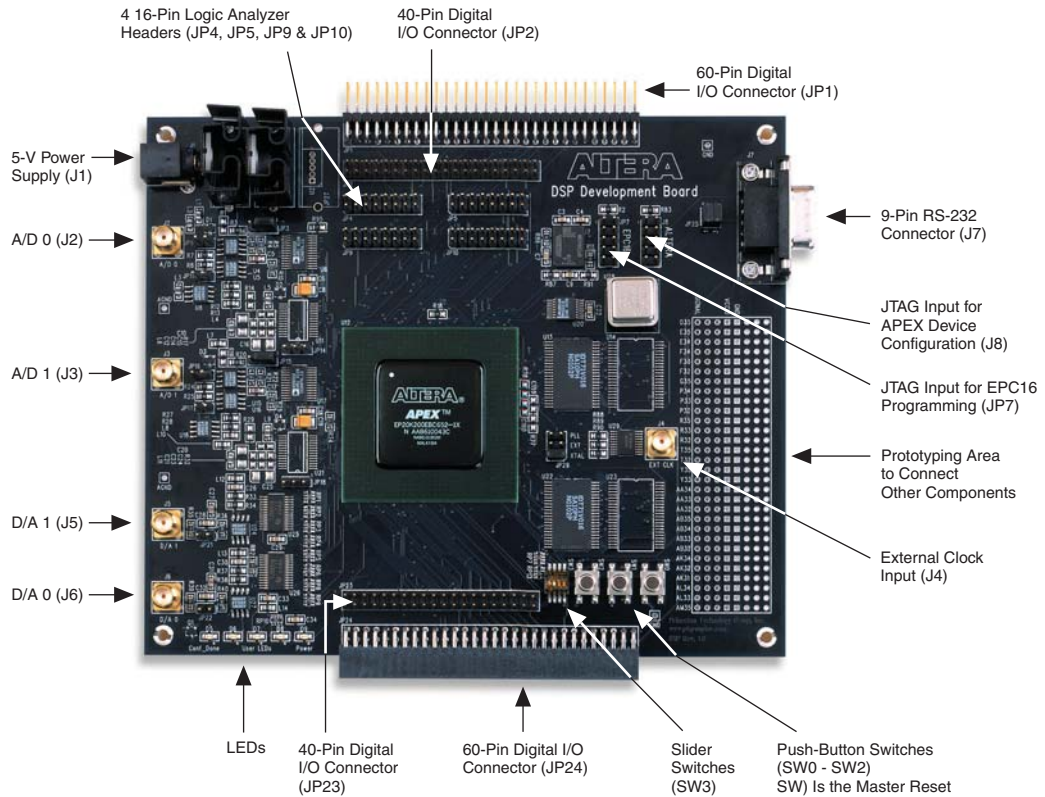
The APEX DSP development board starter version is a development platform that provides system designers with an economical solution for hardware verification. This rapid prototyping board enables the user to debug and verify both functionality and design timing. With two analog input and output channels per board and the ability to combine boards easily with right angle connectors, the APEX DSP development board can be used to construct an extremely powerful processing system. Combined with DSP intellectual property (IP) from Altera and the Altera Megafunction Partners Program (AMPP™) partners, the user can solve design problems that formerly required custom solutions.

APEX DSP Development Board (Starter Version) Data Sheet

The APEX DSP development board starter version includes an APEX EP20K200E-1X device, a 10-bit analog I/O connector, and 256 KBytes of memory.

Figure 1 shows a top view of the board.

Figure 1. APEX DSP Development Board



Interfaces

Table 1 describes the interfaces supported by the board.

Interface	Type	Description
RS-232	I/O	The board has a 9-pin D connector, which can be configured as a DTE or DCE serial port. The interface voltages are converted to 3.3-V signals and brought to the APEX device, which must be configured to generate and accept transmissions.
User I/O pins	I/O	The board has 150 general-purpose I/O pins on the 0.1" headers JP1, JP2, JP23, and JP24.
Debug headers	I/O	The board has 32 general-purpose I/O pins on the .1" headers JP4, JP5, JP9, and JP10. These pins are for use with an external logic analyzer.
Analog SMA connector	Input	The board has 2 SMA connector inputs terminated in 50 Ω .
Analog SMA connector	Output	The board has 2 SMA connector outputs with a source impedance of 50 Ω .
Prototyping area	I/O	The board provides a grid of plated through-holes on 0.1" centers. 30 APEX I/O pins are connected to the grid.

Environmental Requirements

The development board must be stored between -40°C and 100°C . The recommended operating temperature is between 0°C and 55°C .



The board can be damaged without proper anti-static handling. Therefore, you should take anti-static precautions before handling the board.

Using the Board

The board ships programmed with a filtering design. Once power is applied to the board, the POWER ON LED turns on. Next, the EPC16 configures the APEX device; successful configuration is indicated by the CONF_DONE LED turning on.

To configure the board with a new design, the designer should perform the following steps:

1. Apply power.
2. Configure the APEX device.
3. Reset the board.

1. Apply Power

Power should be applied to the board by connecting the 5.0-V DC power supply adapter provided in the DSP kit to connector J1 (see [Figure 1 on page 2](#)). All of the board components are powered either directly from the 5.0-V supply or through 3.3-V and 1.8-V regulators powered from the 5.0-V supply.


- The 3.3-V supply powers the APEX device and LVTTTL board components.
- The 1.8-V supply provides V_{CCINT} to the Altera APEX device.

When power is applied to the board, the POWER ON LED, D9, turns on.

2. Configure the APEX Device


After power-up, the EPC16 configuration device, which ships pre-programmed with a filtering design, automatically configures the APEX 20KE device via a 10-pin header. The CONF_DONE LED turns on signifying that the APEX device is configured.

To change the programming file in the device, the designer can program the EPC16 device with the Quartus® II software and the ByteBlasterMV cable and then turn power to the board off and then on again. Alternatively, the designer can configure the APEX device directly—without turning off the power—using the Quartus II software and the ByteBlasterMV cable.

 The designer can also use the Altera MasterBlaster™ cable to program the EPC16 device or configure the APEX device. However, this cable is not provided with the APEX DSP Development Kit.

Configure the APEX Device with the EPC16 Device

New configuration data can be programmed into the EPC16 configuration device, which configures the APEX device with the new data after power to the board is cycled. The user can program the EPC16 device using the Quartus II software version 2000.02 or higher using the ByteBlasterMV cable connected to JP7 (see [Figure 1 on page 2](#)). In the Quartus II software, select the JTAG mode and indicate which Programmer Object File (.pof) to use for programming.

 Be sure to connect pin 1 of the cable (indicated by a red stripe) to pin 1 of the header on the board. See [Figure 8 on page 21](#) for the pin positions of the board header.



Refer to Quartus II Help for instructions on how to use the ByteBlasterMV cable.

Configure the APEX Device Directly

The Quartus II software version 2000.02 or higher can configure the APEX device directly via the ByteBlasterMV cable without cycling power to the board. The cable connects to JP7 (see [Figure 1 on page 2](#)) on the board. In the Quartus II software, select the JTAG mode and select the SRAM Object File (.sof) generated by the software for configuration.



Be sure to connect pin 1 of the cable (indicated by a red stripe) to pin 1 of the header on the board. See [Figure 8 on page 21](#) for the pin positions of the board header.



Refer to Quartus II Help for instructions on how to use the ByteBlasterMV cable.

3. Reset the Board

The master reset switch, SW0, resets the APEX 20K device through the DEV_CLRn input signal (if this reset mode is selected during compilation). Alternatively, this pin can be used as a standard I/O pin to implement a reset in a design.

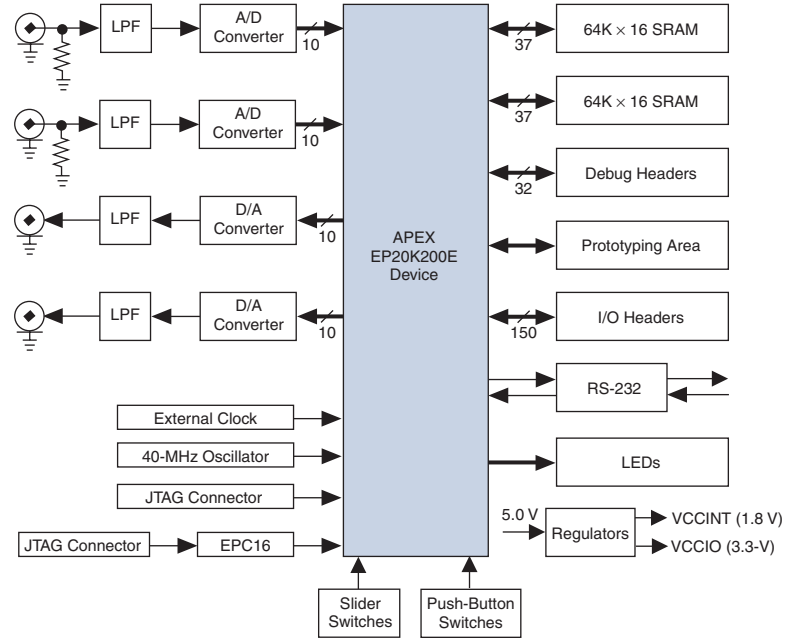


SW0 is not a board-level reset. The APEX device should drive a reset to any devices on the board that must be reset. This process allows devices on the board to be reset independently from the global reset without requiring additional hardware to prevent contention.

Functional Description

This section describes the elements of the DSP development board. [Figure](#) shows a block diagram of the board.

Figure 2. APEX DSP Development Board Starter Version Block Diagram



APEX Device

The EP20K200E-1X device on the starter kit board features 211,000 gates in a 652-pin FineLine BGA™ package. The device has 8,320 logic cells and 106,496 RAM bits.



For more information on APEX devices, go to the [APEX 20K Programmable Logic Device Family Data Sheet](#).

Table 2 describes the APEX device features.

Table 2. APEX Device Features	
Feature	EP20K200EBC652-1X
Maximum gates (logic and RAM)	526,000
Typical gates	200,000
Logic elements (LEs)	8,320
Embedded system blocks (ESBs)	52
Maximum RAM bits	106,496
Maximum macrocells	832
Maximum user I/O pins	382
Internal supply voltage	1.8V
MultiVolt™ I/O interface voltage levels	3.3 V, 2.5 V
Package	652 BGA
I/O count	376
Board reference	U12
Voltage	1.8-V internal, 3.3-V I/O

EPC16 Configuration Device

Table 3 describes the EPC16 device features.

Table 3. EPC16 Reference	
Item	Description
Board reference	U7
Part number	EPC16
Device description	16-Mbit Flash Configuration Device
Voltage	3.3-V
Manufacturer	Altera
Manufacturer web site	http://www.altera.com

A/D Converters

The APEX DSP development board has two A/D converters. The A/D subsystem of the board has the following features:

- The A/D converters produce 10-bit samples at a maximum rate of 40 MSPS.
- The analog input to each A/D converter is single-ended.

- The data output format to each A/D converter is two's complement.
- The voltage input range to each A/D converter is user-selectable at 1 V_{PP} or 2 V_{PP} (1 V_{PP} is the default, see jumpers JP3 and JP15 in [Table 15](#)).
- The input to each A/D converter is user-selectable as AC coupled or DC coupled (AC coupled is the default, see jumpers JP6 and JP16 in [Table 15](#)).
- The analog gain of each A/D converter input is user-selectable (an analog gain = 1 is the default, see jumpers JP11 and JP17 in [Table 15](#)).
- The A/D converter clock is user-selectable and can be the 40-MHz oscillator or an external clock (the 40-MHz oscillator is the default, see Jumper JP29 in [Table 15](#)).
- Provides an out of range (OTR) output bit that indicates when the input signal is beyond the A/D connector's input range.

A signal travels through the A/D converter subsystem in the following manner:

- The analog input enters through SMA connectors with 50-Ohm terminators.
- The signal is AC coupled with a 3-dB frequency of 338 Hz. The AC path can be bypassed if a DC path is desired.
- The signal is buffered with a gain amplifier.
- The signal goes through a low-pass, active, two-pole filter with a 3-dB frequency of 20 MHz. The 3-dB frequency can be adjusted by using different resistors and capacitors. See [“Adjusting the Low-Pass Filter Parameters” on page 16](#) for more information on changing the frequency.

[Table 4](#) lists reference information for the A/D converters.

Table 4. A/D Converter Reference	
Item	Description
Board reference	U6, U17
Part number	AD9203ARU
Device description	10-bit, 40-MSPS A/D converter
Voltage	3.3-V digital V_{DD} , 5.0-V analog V_{DD}
Manufacturer	Analog Devices
Manufacturer web site	http://www.analog.com

D/A Converters

The APEX DSP development board has two D/A converters. The D/A subsystem of the board has the following features:

- The converters produce 10-bit samples at a maximum rate of 100 MSPS.
- The analog output from the D/A converter is single-ended.
- The output from each D/A converter is user selectable as AC coupled or DC coupled (AC coupled is the default, see jumpers JP21 and JP22 in [Table 15](#)).
- The analog output is 0 V to 1 V when DC coupled and -0.5 V to +0.5 V when AC coupled.
- The data input format into the D/A converter is two's complement.
- The D/A converters are clocked from APEX pin CLKLK_OUT2p (see [Figure 3](#)).

A signal travels through the D/A in the following manner:

- D/A outputs are buffered with an amplifier with a gain of two. Then the outputs go through a low-pass, active, two-pole filter with a 3-dB frequency of 20 MHz. The 3-dB frequency can be changed by using different resistors and capacitors. The user can replace the output resistor with a 0-Ohm resistor, which lowers the output impedance and uses the lower 3-dB frequency created by the AC coupled output. Additionally, the output gain can be increased or decreased by changing the resistor connecting the negative input of the output amplifier to ground. Changing the gain also affects the output low-pass filter. See [“Adjusting the Low-Pass Filter Parameters” on page 16](#) for more information on changing the frequency.
- The filter outputs are AC-coupled with a 3-dB frequency of 22.1 KHz, which can be bypassed if a DC path is desired.
- The signal is connected to an SMA connector through a 50-Ohm resistor.

Table 5 lists reference information for the D/A converters.

Table 5. D/A Converter Reference	
Item	Description
Board reference	U25, U26
Part number	THS5651AIPW
Device description	10-bit, 100-MSPS D/A converter
Voltage	3.3-V digital V_{DD} , 5.0-V analog V_{DD}
Manufacturer	Texas Instruments
Manufacturer web site	http://www.ti.com

Voltage Amplifiers

Operational amplifiers are used in the input and output analog circuitry. Table 6 lists reference information for the rail-to-rail voltage amplifiers.

Table 6. Rail-to-Rail Voltage Amplifier Reference	
Item	Description
Board reference	A/D 0: U4, U5, U8. A/D 1: U15, U16, U18. D/A 0 and D/A 1: U24, U27
Part number	AD8061AR
Device description	Rail-to-Rail voltage amplifiers
Voltage	5.0 V
Manufacturer	Analog Devices
Manufacturer web site	http://www.analog.com

Clocks & Clock Distribution

The board has a 40-MHz oscillator, which drives the APEX device CLK1P and CLK2P inputs. An external user-supplied input on an SMA connector can also be used as a clock source driving the APEX device CLK3P and CLK4P inputs. These clocks can be used to drive the A/D converters directly. The D/A converters are driven from CLKLK_OUT2p, which provides flexibility in the conversion rate.

The board's clock distribution technique is shown in Figure 3. The APEX device receives both the on-board 40-MHz clock and the external clock, which is brought in on J4 and terminated in 50 Ω . Each clock connects to two clock inputs on the APEX device. Therefore, each clock can be routed to the device's phase-locked loop output, which clocks the converters.

The 40-MHz crystal clock and the external clock connect to the A/D converters. A jumper on JP29 selects the source clock for the A/D converter.

Figure 3. Clock Distribution

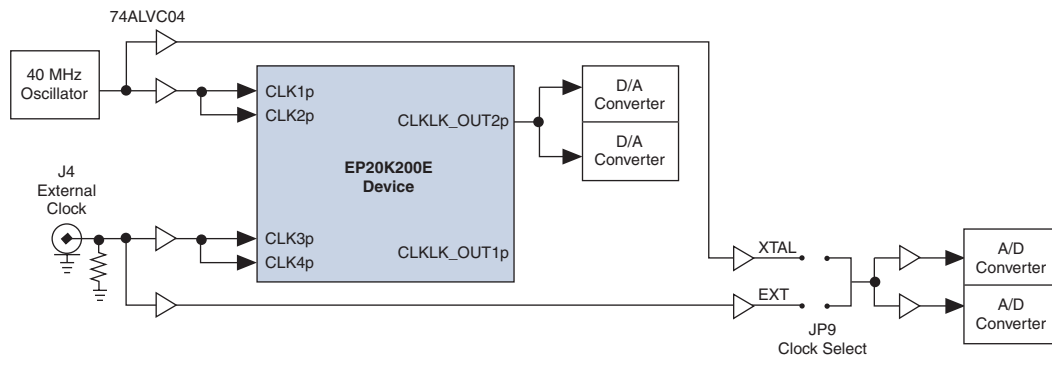


Table 7 lists reference information for the external clock.

Table 7. External Clock Reference	
Item	Description
Board reference	U28
Part number	40MHz OSC
Device description	Oscillator
Manufacturer	Raltron
Manufacturer web site	http://www.raltron.com

Memory

The board has two banks of 12-ns asynchronous 64K × 16 SRAM. The SRAM can be used independently or combined to have a 32-bit wide organization.

In addition to address and data lines, each 16-bit-wide bank is controlled by write enable (/WE), output enable (/OE), byte high enable (/BHE), and byte low enable (/BLE) signals, and each device has its own chip enable (/CE).

Table 8 lists the characteristics of the SRAM memories and the configuration device on the board.

Type	Address Lines	Data Lines	Memory Organization	Size (KBytes)	I/O Pins Used	Power (mW)
SRAM 0	16	16	64K × 16	128	37	660
SRAM 1	16	16	64K × 16	128	37	660

Table 9 lists reference information for the SRAM memories.

Item	Description
Board reference	U13, U14, U22, U23
Part number	IDT71V016SA
Device description	3.3-V, 12-ns 64K × 16 SRAM
Manufacturer	IDT
Manufacturer web site	http://www.idt.com

Figure 4 shows a block diagram of the APEX device memory architecture.

Figure 4. APEX Device Memory Architecture

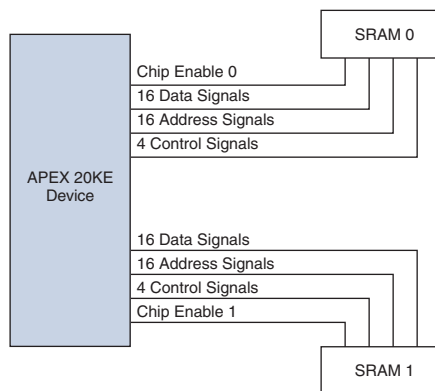


Figure 5.

Power

The eight-layer development board has four signal layers, a split 3.3-V, 5.0-V power plane, a split 1.8-V ground plane, and two additional split ground planes. The board is powered from a single, well-regulated 5.0-V supply.

Regulators on board are used to develop the V_{CCINT} (1.8 V) and V_{CCIO} (3.3 V) voltages. The board includes a POWER ON LED that indicates the presence of V_{CCIO} .

The following board elements are 3.3 V:

- LEDs
- Switches
- Crystal oscillator

Tables 10 and 11 show the specifications of the power elements on the board.

Table 10. Power Reference for 3.3-V V_{CCIO}

Item	Description
Board reference	U1
Part number	MIC2940-3.3BT
Device description	1.2-Amp Programmable Low Dropout Regulator (3.3 V on board)
Manufacturer	Micrel
Manufacturer web site	http://www.micrel.com

Table 11. Power Reference for V_{CCINT}

Item	Description
Board reference	U3
Part number	MIC2941ABT
Device description	1.8-V, 1.2-Amp Programmable Low Dropout Regulator
Manufacturer	Micrel
Manufacturer web site	http://www.micrel.com

Serial Interface

The board contains a DB9 connector, which provides a bidirectional RS-232C serial I/O interface. The board contains the transceiver; however, the APEX device must implement the logic controller. The interface can be configured with a jumper as either data terminal equipment (DTE) or data communications equipment (DCE) using JP25. [Table 12](#) describes the device used to implement the RS-232C interface.

Table 12. RS-232C Interface Device Reference	
Item	Description
Board reference	U20
Part number	MAX3221ECAE
Device description	RS-232 transceiver
Voltage	3.3 V
Manufacturer	Maxim
Manufacturer web site	http://www.maxim-ic.com

Digital Interfaces

The board has 150 digital I/O signals—available on the four 0.1" headers JP1, JP2, JP23, and JP24—connected directly to the APEX device. Additionally, the connector contains many ground signals to ensure the integrity of the signals.

JP1 and JP24 are a matched pair of right-angle connectors, which allow the user to join two DSP boards together by connecting the JP1 connector on one board to the JP24 connector on another. Similarly, JP2 and JP23 can be connected on adjacent boards using a short flat cable terminated with 0.1" headers. Alternatively, JP1, JP2, JP23, and JP24 can be connected to external circuits using flat cables terminated with 0.1" headers. In this case, a cable with male-to-male 0.1" headers must be connected to the two female headers JP23 and JP24. See [“Digital Connector Pinouts” on page 21](#) for pin-out information.



When connecting these pins to external circuitry, the user must adhere to the voltage restrictions specified in the *APEX 20KE Programmable Logic Device Family Data Sheet*. Specifically, the I/O pins are not 5.0-V tolerant and should not be directly connected to logic powered from a 5.0 V supply.

Switch Inputs

The board has four slide switches and three push-button switches, which the user can define as logic inputs. Each push-button signal is defined as a logic 1 when unpressed; when pressed it becomes a logic 0. Each slide switch is defined as a logic 1 when the slide button is closer to the edge of the board; otherwise it is defined as a logic 0.

Logic Analyzer Interface

The board has 32 digital I/O signals—which are available on the four 16-pin 0.1" headers JP4, JP5, JP9, and JP10—connected directly to the APEX device. Each header contains one 8-pin row of signals and one 8-pin row of grounds to attach easily to an external logic analyzer.

Prototyping Area

The board provides room for adding user-selected electronic components. The area is a grid of plated through-holes on 0.1" centers. 30 APEX I/O pins are connected to the inside column of pins in the grid. These pins are labeled on the board for easy identification. One column of ground pins and one column of 3.3-V V_{CCIO} pins provide power to the grid.

Adjusting the Low-Pass Filter Parameters

Both the A/D and D/A converters incorporate active two-pole Sallen-Key low-pass filters in their analog paths set for a 3-db frequency of 20 MHz. An example schematic of the type used in the D/A converter is shown in [Figure 6](#).

The transfer function (V_{OUT}/V_{IN}) of the circuit shown is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{1}{S^2 R_1 R_2 C_1 C_2 + SC_2(R_1 + R_2) + SC_1 R_1(1 - K) + 1}$$

where $S = j2\pi f$, f is the frequency, and K is the closed-loop gain of the operating amp combined with R_F and R_{GAIN} as shown in the equation:

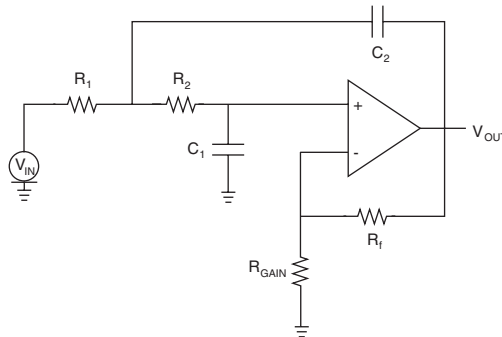
$$K = \frac{R_F + R_{GAIN}}{R_{GAIN}}$$

Defining f_0 as the 3-db filter frequency and ζ as the damping factor gives the following equations:

$$f_0 = \frac{1}{2\pi(R_1 R_2 C_1 C_2)^{1/2}}$$

$$\zeta = \frac{C_2(R_1 + R_2) + C_1 R_1(1 - K)}{2(R_1 R_2 C_1 C_2)}$$

Figure 6. D/A Sallen-Key Low Pass Filter



The filters in the D/A circuits have a 3-db bandwidth of 20-MHz and a damping factor of 0.707. This damping factor provides a flat frequency response with no peaking. Table 13 shows the values used on the board; if the user wants to change the characteristics of either filter, the resistors and capacitors should be replaced according to the formulae above.

Board Element	R ₁	R ₂	C ₁	C ₂	R _f	R _{GAIN}
D/A 0	R37 + R61 100 Ω	R38 200 Ω	C154 56 pf	C31 56 pf	R40 100 Ω	R63 100 Ω
D/A 1	R33 + R57 100 v	R34 200 v	C27 56 pf	C145 56 pf	R36 100 Ω	R59 100 Ω

Figure 7 shows a schematic of the filters used with the A/D converters. The transfer function (V_{OUT}/V_{IN}) of the circuit is:

$$\frac{V_{OUT}}{V_{IN}} = \frac{(R_F + R_{GAIN})/R_{GAIN}}{S^2 R_1 R_2 C_1 C_2 + S C_2 (R_1 + R_2) + 1}$$

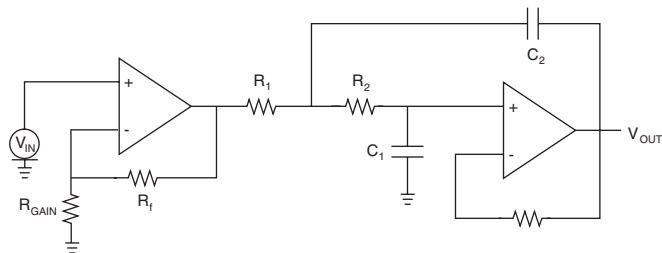
where $S = j2\pi f$ and f = the frequency.

Defining f_0 as the 3-db filter frequency and ζ as the damping factor gives the following equations:

$$f_0 = \frac{1}{2\pi(R_1 R_2 C_1 C_2)^{1/2}}$$

$$\zeta = \frac{C_2(R_1 + R_2)}{2(R_1 R_2 C_1 C_2)^{1/2}}$$

Figure 7. A/D Amplifier & Sallen-Key Low-Pass Filter



The filters in the A/D circuits have a 3-db bandwidth of 20-MHz and a damping factor of 0.707. This damping factor provides a flat frequency response with no peaking. Table 14 shows the values used on the board; if the user wants to change the characteristics of either filter, the resistors and capacitors should be replaced according to the formulae above.

Table 14. A/D Filter Component Values

Board Element	R₁	R₂	C₁	C₂	R_f	R_{GAIN}
A/D 0	R4 100 Ω	R5 100 Ω	C45 110 pf	C5 56 pf	R3 100 Ω	R1 100 Ω
A/D 1	R21 100 Ω	R22 100 Ω	C82 110 pf	C17 56 pf	R20 100 Ω	R19 100 Ω

Jumper Settings

The DSP development board has several analog and digital jumper options, which are given in [Table 15](#) ordered by jumper number.

Number	Function	Setting (1)	Option Selected
JP3	A/D 0 Range Select	1 to 2 (2) 2 to 3	1 V_{PP} 2 V_{PP}
JP6	A/D 0 AC/DC Select	Not Jumpered (2) Jumpered	AC Coupled DC Coupled
JP11	A/D 0 Gain Select	Not Jumpered (2) Jumpered	Analog Gain = 1 Analog Gain = $1 + 100/R_{GAIN}$ (Labeled R1 on the board)
JP15	A/D 1 Range Select	1 to 2 (2) 2 to 3	1 V_{PP} 2 V_{PP}
JP16	A/D 1 AC/DC Select	Not Jumpered (2) Jumpered	AC Coupled DC Coupled
JP17	A/D 1 Gain Select	Not Jumpered (2) Jumpered	Analog Gain = 1 Analog Gain = $1 + 100/R_{GAIN}$ (Labeled R19 on the board)
JP21	D/A 1 AC/DC Select	Not Jumpered (2) Jumpered	AC Coupled DC Coupled
JP22	D/A 0 AC/DC Select	Not Jumpered (2) Jumpered	AC Coupled DC Coupled
JP25	DTE/DCE Select	1-2, 3-4 (2) 1-3, 2-4	RS-232 DTE Configuration RS-232 DCE Configuration
JP29	A/D Clock Select	XTAL EXT	AtoD Clock from 40-MHz Crystal AtoD Clock from External Clock

Note:

- (1) For jumpers with three pins, pin 1 on the board is labeled above the jumpers.
- (2) This jumper setting is the factory default setting.

Input/Output Connections

The board has several analog and digital input and output connections.

Analog I/O

The analog I/O pins and connectors are described in [Table 16](#).

Connector	Signal
J2	A/D 0 Input Connector
J3	A/D 1 Input Connector
J5	D/A 1 Output Connector
J6	D/A 0 Output Connector

Digital I/O

The digital I/O pins and connectors are described in [Table 17](#).

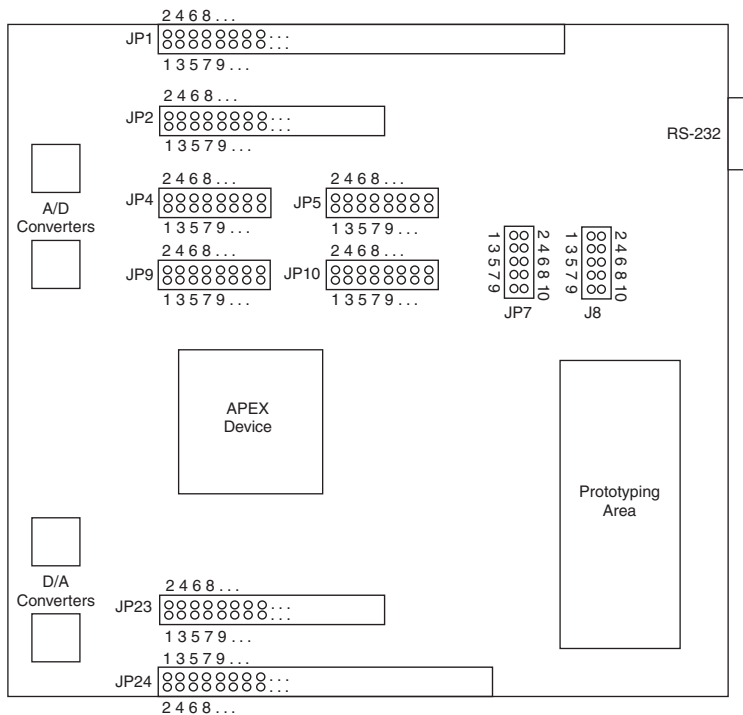
Connector	Signal
J4	External Clock Input
J7	RS-232 DB9 Connector (9 Pins)
JP1	Digital I/O Connector (60 Pins)
JP2	Digital I/O Connector (40 Pins)
JP4	Logic Analyzer Header (16 Pins)
JP5	Logic Analyzer Header (16 Pins)
JP7	JTAG Input for EPC16 Programming
J8	JTAG Input for APEX Configuration
JP9	Logic Analyzer Header (16 Pins)
JP10	Logic Analyzer Header (16 Pins)
JP23	Digital I/O Connector (40 Pins)
JP24	Digital I/O Connector (60 Pins)
-	Prototyping Area (90 Pins)

Digital Connector Pinouts

Figure 8 shows the position of the pins on the board.

Figure 8. Pin Positions

Board is not drawn to scale.



The J7 pin-out for the RS-232 DB9 connector is shown below:

- Transmit with JP25 1-2, 3-4 jumpered. Receive with JP25 1-3, 2-4 jumpered.
- Receive with JP25 1-3, 2-4 jumpered. Transmit with JP25 1-2, 3-4 jumpered.
- Ground.

The prototyping area has the pins shown in Table 18, which connect to the APEX device.



Some of the pin names are marked on the the development board incorrectly. Refer to [Table 18](#), not the board, for the correct pinout.

Table 18. Prototyping Area Pinout

Prototyping Pin	APEX Pin	Label on Board
1	H35	D35
2	H34	E35
3	H33	E34
4	H32	F34
5	H31	F32
6	H30	G35
7	J35	P34
8	T32	P33
9	T31	P32
10	T30	R35
11	Y35	R33
12	Y33	R32
13	Y31	T35
14	AA34	T32
15	AA33	Y35
16	AA32	Y33
17	AA30	AA34
18	AB35	AA33
19	AB34	AA32
20	AB33	AB35
21	AB32	AB34
22	AB31	AB33
23	AB30	AB32
24	AC35	AC35
25	AK34	AK34
26	AK32	AK32
27	AK31	AK31
28	AL34	AL34
29	AL33	AL33
30	AM35	AM35

The pin assignments for the digital I/O connectors are given in [Tables 19](#) through [28](#).

Table 19. JP1 Pin-Out (Digital I/O Connector) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP1-1	I/OT_1	D21	JP1-31	I/OT_38	A26
JP1-2	I/OT_0	B26	JP1-32	GND	N.C.
JP1-3	I/OT_2	A8	JP1-33	I/OT_41	B11
JP1-4	GND	N.C.	JP1-34	I/OT_42	E16
JP1-5	I/OT_4	A10	JP1-35	I/OT_44	B12
JP1-6	I/OT_3	D22	JP1-36	GND	N.C.
JP1-7	I/OT_5	D23	JP1-37	I/OT_47	B13
JP1-8	GND	N.C.	JP1-38	I/OT_48	E21
JP1-9	I/OT_7	C12	JP1-39	I/OT_50	B14
JP1-10	I/OT_6	A11	JP1-40	GND	N.C.
JP1-11	I/OT_10	A13	JP1-41	I/OT_53	B15
JP1-12	GND	N.C.	JP1-42	I/OT_54	E23
JP1-13	I/OT_13	A14	JP1-43	I/OT_56	B16
JP1-14	I/OT_12	C14	JP1-44	GND	N.C.
JP1-15	I/OT_16	A15	JP1-45	I/OT_59	B20
JP1-16	GND	N.C.	JP1-46	I/OT_60	D14
JP1-17	I/OT_19	A16	JP1-47	I/OT_62	B21
JP1-18	I/OT_18	C16	JP1-48	GND	N.C.
JP1-19	I/OT_22	A20	JP1-49	I/OT_65	B22
JP1-20	GND	N.C.	JP1-50	I/OT_66	D16
JP1-21	I/OT_25	A21	JP1-51	I/OT_68	B23
JP1-22	I/OT_24	C21	JP1-52	GND	N.C.
JP1-23	I/OT_28	E13	JP1-53	I/OT_69	D20
JP1-24	GND	N.C.	JP1-54	I/OT_70	G33
JP1-25	I/OT_31	C25	JP1-55	I/OT_71	B24
JP1-26	I/OT_30	C24	JP1-56	GND	N.C.
JP1-27	I/OT_34	E14	JP1-57	I/OT_72	G32
JP1-28	GND	N.C.	JP1-58	I/OT_73	B25
JP1-29	I/OT_37	E15	JP1-59	I/OT_74	G31
JP1-30	I/OT_36	A25	JP1-60	GND	N.C.

Table 20. JP2 Pin-Out (Digital I/O Connector) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP2-1	I/OT_9	C13	JP2-21	I/OT_39	B7
JP2-2	I/OT_8	A12	JP2-22	I/OT_40	A27
JP2-3	I/OT_11	E2	JP2-23	I/OT_43	A28
JP2-4	GND	N.C.	JP2-24	GND	N.C.
JP2-5	I/OT_15	C15	JP2-25	I/OT_45	E20
JP2-6	I/OT_14	E1	JP2-26	I/OT_46	D35
JP2-7	I/OT_17	D1	JP2-27	I/OT_49	E35
JP2-8	GND	N.C.	JP2-28	GND	N.C.
JP2-9	I/OT_21	C20	JP2-29	I/OT_51	E22
JP2-10	I/OT_20	C1	JP2-30	I/OT_52	E34
JP2-11	I/OT_23	E7	JP2-31	I/OT_55	F34
JP2-12	GND	N.C.	JP2-32	GND	N.C.
JP2-13	I/OT_27	A22	JP2-33	I/OT_57	D13
JP2-14	I/OT_26	C22	JP2-34	I/OT_58	F33
JP2-15	I/OT_29	C23	JP2-35	I/OT_61	F32
JP2-16	GND	N.C.	JP2-36	GND	N.C.
JP2-17	I/OT_33	A24	JP2-37	I/OT_63	D15
JP2-18	I/OT_32	A23	JP2-38	I/OT_64	G35
JP2-19	I/OT_35	B5	JP2-39	I/OT_67	G34
JP2-20	GND	N.C.	JP2-40	GND	N.C.

Table 21. JP4 Pin-Out (Logic Analyzer Header) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP4-1	DEBUG8	AF1	JP4-9	DEBUG12	AF3
JP4-2	GND	N.C.	JP4-10	GND	N.C.
JP4-3	DEBUG9	H2	JP4-11	DEBUG13	G5
JP4-4	GND	N.C.	JP4-12	GND	N.C.
JP4-5	DEBUG10	AF2	JP4-13	DEBUG14	AF4
JP4-6	GND	N.C.	JP4-14	GND	N.C.
JP4-7	DEBUG11	G6	JP4-15	DEBUG15	G4
JP4-8	GND	N.C.	JP4-16	GND	N.C.

Table 22. JP5 Pin-Out (Logic Analyzer Header) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP5-1	DEBUG16	AF5	JP5-9	DEBUG20	AG2
JP5-2	GND	N.C.	JP5-10	GND	N.C.
JP5-3	DEBUG17	G3	JP5-11	DEBUG21	G1
JP5-4	GND	N.C.	JP5-12	GND	N.C.
JP5-5	DEBUG18	AF6	JP5-13	DEBUG22	AG3
JP5-6	GND	N.C.	JP5-14	GND	N.C.
JP5-7	DEBUG19	G2	JP5-15	DEBUG23	F6
JP5-8	GND	N.C.	JP5-16	GND	N.C.

Table 23. JP7 Pin-Out (JTAG) Note (1)

I/O Pin	Signal Name	EPC16 Pin	I/O Pin	Signal Name	EPC16 Pin
JP7-1	TCK	C2	JP7-6	VCCIO	N.C.
JP7-2	GND	N.C.	JP7-7	-	-
JP7-3	TD0	E2	JP7-8	-	-
JP7-4	VCCIO	N.C.	JP7-9	TDI	D2
JP7-5	TMS	F2	JP7-10	GND	N.C.

Table 24. JP8 Pin-Out (ByteBlasterMV) Note (1)

I/O Pin	Signal Name	I/O Pin	Signal Name
JP8-1	TCK	JP8-6	VCCIO
JP8-2	GND	JP8-7	-
JP8-3	TD0	JP8-8	-
JP8-4	VCCIO	JP8-9	TDI
JP8-5	TMS	JP8-10	GND

Table 25. JP9 Pin-Out (Logic Analyzer Header) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP9-1	DEBUG0	AE3	JP9-9	DEBUG4	AE5
JP9-2	GND	N.C.	JP9-10	GND	N.C.
JP9-3	DEBUG1	J1	JP9-11	DEBUG5	H4
JP9-4	GND	N.C.	JP9-12	GND	N.C.
JP9-5	DEBUG2	AE4	JP9-13	DEBUG6	AE6
JP9-6	GND	N.C.	JP9-14	GND	N.C.
JP9-7	DEBUG3	H6	JP9-15	DEBUG7	H3
JP9-8	GND	N.C.	JP9-16	GND	N.C.

Table 26. JP10 Pin-Out (Logic Analyzer Header) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP10-1	DEBUG24	AG4	JP10-9	DEBUG28	AG6
JP10-2	GND	N.C.	JP10-10	GND	N.C.
JP10-3	DEBUG25	F5	JP10-11	DEBUG29	F2
JP10-4	GND	N.C.	JP10-12	GND	N.C.
JP10-5	DEBUG26	AG5	JP10-13	DEBUG30	AH1
JP10-6	GND	N.C.	JP10-14	GND	N.C.
JP10-7	DEBUG27	F4	JP10-15	DEBUG31	F1
JP10-8	GND	N.C.	JP10-16	GND	N.C.

Table 27. JP23 Pin-Out (Digital I/O Connector) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP23-1	I/OB_9	AL23	JP23-21	I/OB_39	AN13
JP23-2	I/OB_8	AP20	JP23-22	I/OB_40	AK1
JP23-3	I/OB_11	AM13	JP23-23	I/OB_43	AK2
JP23-4	GND	N.C.	JP23-24	GND	N.C.
JP23-5	I/OB_15	AM15	JP23-25	I/OB_45	AN15
JP23-6	I/OB_14	AP23	JP23-26	I/OB_46	AK3
JP23-7	I/OB_17	AH6	JP23-27	I/OB_49	AK4
JP23-8	GND	N.C.	JP23-28	GND	N.C.
JP23-9	I/OB_21	AM20	JP23-29	I/OB_51	AN20
JP23-10	I/OB_20	AJ1	JP23-30	I/OB_52	AK5
JP23-11	I/OB_23	AJ2	JP23-31	I/OB_55	AK6
JP23-12	GND	N.C.	JP23-32	GND	N.C.
JP23-13	I/OB_27	AM22	JP23-33	I/OB_57	AN22
JP23-14	I/OB_26	AJ3	JP23-34	I/OB_58	AL1
JP23-15	I/OB_29	AJ4	JP23-35	I/OB_61	AM1
JP23-16	GND	N.C.	JP23-36	GND	N.C.
JP23-17	I/OB_33	AN11	JP23-37	I/OB_63	AN24
JP23-18	I/OB_32	AJ5	JP23-38	I/OB_64	AL13
JP23-19	I/OB_35	AJ6	JP23-39	I/OB_67	AL14
JP23-20	GND	N.C.	JP23-40	GND	N.C.

Table 28. JP24 Pin-Out (Digital I/O Connector) (Part 1 of 2) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP24-1	I/OB_1	AL16	JP24-31	I/OB_38	AR13
JP24-2	I/OB_0	AP13	JP24-32	GND	N.C.
JP24-3	I/OB_2	AP14	JP24-33	I/OB_41	AR14
JP24-4	GND	N.C.	JP24-34	I/OB_42	AN14
JP24-5	I/OB_4	AP15	JP24-35	I/OB_44	AR15
JP24-6	I/OB_3	AL20	JP24-36	GND	N.C.
JP24-7	I/OB_5	AL21	JP24-37	I/OB_47	AR16
JP24-8	GND	N.C.	JP24-38	I/OB_48	AN16
JP24-9	I/OB_7	AL22	JP24-39	I/OB_50	AR20
JP24-10	I/OB_6	AP16	JP24-40	GND	N.C.
JP24-11	I/OB_10	AP21	JP24-41	I/OB_53	AR21
JP24-12	GND	N.C.	JP24-42	I/OB_54	AN21

Table 28. JP24 Pin-Out (Digital I/O Connector) (Part 2 of 2) Note (1)

I/O Pin	Signal Name	APEX Pin	I/O Pin	Signal Name	APEX Pin
JP24-13	I/OB_13	AM14	JP24-43	I/OB_56	AR22
JP24-14	I/OB_12	AP22	JP24-44	GND	N.C.
JP24-15	I/OB_16	AP24	JP24-45	I/OB_59	AR23
JP24-16	GND	N.C.	JP24-46	I/OB_60	AN23
JP24-17	I/OB_19	AP25	JP24-47	I/OB_62	AR24
JP24-18	I/OB_18	AM16	JP24-48	GND	N.C.
JP24-19	I/OB_22	AP26	JP24-49	I/OB_65	AR25
JP24-20	GND	N.C.	JP24-50	I/OB_66	AN25
JP24-21	I/OB_25	AR8	JP24-51	I/OB_68	AR26
JP24-22	I/OB_24	AM21	JP24-52	GND	N.C.
JP24-23	I/OB_28	AR9	JP24-53	I/OB_69	AP10
JP24-24	GND	N.C.	JP24-54	I/OB_70	AL15
JP24-25	I/OB_31	AR10	JP24-55	I/OB_71	AR27
JP24-26	I/OB_30	AM23	JP24-56	GND	N.C.
JP24-27	I/OB_34	AR11	JP24-57	I/OB_72	AP11
JP24-28	GND	N.C.	JP24-58	I/OB_73	AR28
JP24-29	I/OB_37	AR12	JP24-59	I/OB_74	AP12
JP24-30	I/OB_36	AN12	JP24-60	GND	N.C.

Note to tables:

(1) N.C. = no connect.

APEX On-Board Interfaces

Tables 29 through 40 give the pin assignments for the APEX digital interfaces to the A/D and D/A converters and RAM.

Table 29. LED APEX Pin-Puts

Signal Name	APEX Pin
LED0	AH5
LED1	AH3
LED2	AH2

Table 30. Push-Button Switch APEX Pin-Outs

Signal Name	APEX Pin
SWITCH0	T6
SWITCH1	T1
SWITCH2	R6

Table 31. Slide Switch APEX Pin-Outs

Signal Name	Board Name	APEX Pin
SWITCH6	SW3 Pin 1	P5
SWITCH5	SW3 Pin 2	P6
SWITCH4	SW3 Pin 3	R1
SWITCH3	SW3 Pin 4	R2

Table 32. Clock APEX Pin-Outs

Signal Name	APEX Pin	APEX Global Name
CLK1 (oscillator)	W34	Clk1p
	U2	Clk2p
CLK (external)	Y34	Clk3p
	T2	Clk4p

Table 33. A/D 0 & A/D 1 APEX Pin-Outs

Signal Name	A/D 0 APEX Pin	A/D 1 APEX Pin
OTR	K1	M3
AD [9] (MSB)	K4	M6
AD [8]	K5	N1
AD [7]	K6	N2
AD [6]	L1	N3
AD [5]	L2	N5
AD [4]	L4	N6
AD [3]	L5	P1
AD [2]	L6	P2
AD [1]	M1	P3
AD [0] (LSB)	M2	P4

Table 34. D/A 0 & D/A 1 APEX Pin-Outs

Signal Name	D/A 0 APEX Pin	D/A 1 APEX Pin
DTOA [13] (MSB)	AB5	T5
DTOA [12]	AB6	W5
DTOA [11]	AC1	Y4
DTOA [10]	AC2	Y5
DTOA [9]	AC4	Y6
DTOA [8]	AC5	AA1
DTOA [7]	AC6	AA2
DTOA [6]	AD1	AA3
DTOA [5]	AD2	AA5
DTOA [4] (LSB)	AD3	AA6

Table 35. SRAM Bank 0 Data Bus Assignments

Signal Name	APEX Pin
SRAM_IO_15	J34
SRAM_IO_14	J33
SRAM_IO_13	J32
SRAM_IO_12	J31
SRAM_IO_11	J30
SRAM_IO_10	K35
SRAM_IO_9	K34
SRAM_IO_8	K33
SRAM_IO_7	K32
SRAM_IO_6	K30
SRAM_IO_5	L35
SRAM_IO_4	L34
SRAM_IO_3	L33
SRAM_IO_2	L32
SRAM_IO_1	L31
SRAM_IO_0	L30

Table 36. SRAM Bank 0 Address Bus Assignments

Signal Name	APEX Pin
SRAM_ADD_15	N33
SRAM_ADD_14	N32
SRAM_ADD_13	N31
SRAM_ADD_12	N30
SRAM_ADD_11	P35
SRAM_ADD_10	P34
SRAM_ADD_9	P33
SRAM_ADD_8	P32
SRAM_ADD_7	P31
SRAM_ADD_6	P30
SRAM_ADD_5	R35
SRAM_ADD_4	R33
SRAM_ADD_3	R32
SRAM_ADD_2	R31
SRAM_ADD_1	R30
SRAM_ADD_0	T35

Table 37. SRAM Bank 0 Control Signal Pin Assignments

Signal Name	APEX Pin
/CS0	M35
/OE0	M32
/WE0	M33
/BHE0	M31
/BLE0	N34

Table 38. SRAM Bank 1 Data Bus Assignments

Signal Name	APEX Pin
SRAM_IO_15	AC34
SRAM_IO_14	AC33
SRAM_IO_13	AC31
SRAM_IO_12	AC30
SRAM_IO_11	AD35
SRAM_IO_10	AD34
SRAM_IO_9	AD33
SRAM_IO_8	AD32
SRAM_IO_7	AD31
SRAM_IO_6	AD30
SRAM_IO_5	AE35
SRAM_IO_4	AE34
SRAM_IO_3	AE32
SRAM_IO_2	AE31
SRAM_IO_1	AE30
SRAM_IO_0	AF35

Table 39. SRAM Bank 1 Address Bus Assignments

Signal Name	APEX Pin
SRAM_ADD_15	AG34
SRAM_ADD_14	AG33
SRAM_ADD_13	AG32
SRAM_ADD_12	AG31
SRAM_ADD_11	AG30
SRAM_ADD_10	AH34
SRAM_ADD_9	AH33
SRAM_ADD_8	AH32
SRAM_ADD_7	AH30
SRAM_ADD_6	AJ35
SRAM_ADD_5	AJ34
SRAM_ADD_4	AJ33
SRAM_ADD_3	AJ32
SRAM_ADD_2	AJ31
SRAM_ADD_1	AJ30
SRAM_ADD_0	AK35

Table 40. SRAM Bank 1 Control Signal Pin Assignments

Signal Name	APEX Pin
/CS1	AF34
/OE1	AF31
/WE1	AF32
/BHE1	AF30
/BLE1	AG35

Revision History

Table 41 shows the document revision history.

<i>Table 41. Revision History</i>	
Date	Description
September 2001, v1.0	First publication.
November 2001, v1.1	Removed references to JP20 from Table 15. Removed information about external clocking in the D/A section.
March 2002, v1.2	Updated SRAM_ADD_14 APEX pin assignment.
April 2002, v1.3	Updated the pinout for the prototyping area.
June 2002, v1.4	Updated pinouts for JP23 in Figure 8 on page 21 .



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