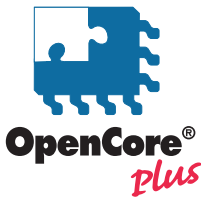


Introduction

Altera offers a broad portfolio of MegaCore® functions, reusable blocks of intellectual property (IP) that can be customized and dropped into a design, allowing you to concentrate on adding proprietary value to your design. All MegaCore functions are fully parameterizable through Altera's unique MegaWizard® Plug-In Manager and are delivered in encrypted format.

The OpenCore® feature lets you test-drive Altera MegaCore functions for free using the Quartus® II or MAX+PLUS® II software. You can verify the functionality of a MegaCore function quickly and easily, as well as evaluate its size and speed before making a purchase decision. However, you cannot generate device programming files.



The OpenCore Plus feature set supplements the OpenCore evaluation flow by incorporating free RTL simulation and hardware evaluation. The OpenCore Plus RTL simulation feature allows you to simulate an RTL model of your MegaCore function in your design. The OpenCore Plus hardware evaluation feature allows you to generate time-limited programming files for a design that includes Altera MegaCore functions. You can use the OpenCore Plus hardware evaluation feature to perform board-level design verification before deciding to purchase licenses for the MegaCore functions. You only need to purchase a license when you are completely satisfied with a core's functionality and performance, and would like to take your design to production.

This application note covers the following topics:

- About OpenCore Plus Hardware Evaluation
- OpenCore Plus Licensing
- Getting Started

About OpenCore Plus Hardware Evaluation

The OpenCore Plus hardware evaluation versions of the MegaCore functions are functionally equivalent to the standard versions, except:

- The OpenCore Plus hardware evaluation versions operate for only a predetermined number of clock cycles, after which the core is disabled in a predefined manner.
- One extra output signal, `timed_out`, switches from low to high when the core has been disabled.



Refer to the *OpenCore Plus Hardware Evaluation with the APEX DSP Development Kit White Paper* for clock cycle limits and the disable behavior of the DSP MegaCore functions provided with the kit.

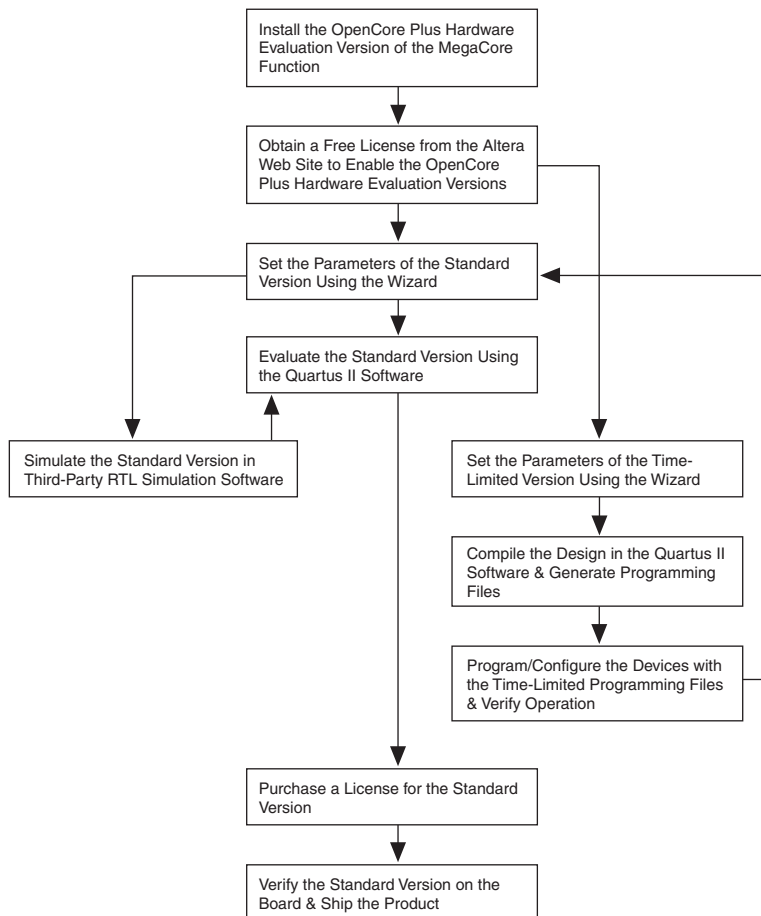
The time-out logic uses approximately 100 logic elements and runs at over 150 MHz. Therefore, it should not limit the performance of most designs.

MegaCore functions that support the OpenCore Plus hardware evaluation feature have an additional library that contains the time-limited versions of all source files required for compilation. For this reason, two sets of source files install in the installation directory for each MegaCore function:

- *lib*—Standard library, which contains source files for the standard version of the core. This version is not time-limited; however, using this library, you cannot generate programming files without first purchasing a license.
- *lib_time_limited*—Time-limited library, which contains time-limited source files for the OpenCore Plus hardware evaluation version of the core. This version times out after a predefined number of clock cycles. You must obtain a free license from the Altera web site to use this version for generating programming files.

When you compile one or more time-limited MegaCore functions in your design, the free OpenCore Plus license allows you to generate a Programmer Object File (.**po**f) or SRAM Object File (.**so**f), which you can use to program an Altera device. After programming a device, the MegaCore function(s) operates normally for a predetermined number of clock cycles, after which the output signals from the function generate a constant known signal instead of their designed functionality. When the function has timed-out, you must reprogram or reconfigure the Altera device to reset the function and continue hardware verification. [Figure 1](#) shows the OpenCore Plus design flow.

Figure 1. OpenCore Plus Design Flow



OpenCore Plus Licensing

You must request a license file from the Altera web site to enable the OpenCore Plus feature. Your license file is sent to you via e-mail; follow the instructions given in the e-mail to install the license.



The OpenCore Plus license allows you to generate programming files, but does not allow you to generate Verilog HDL (.vo) or VHDL (.vho) gate-level netlist files.

The license file enables the compilation of the time-limited versions in the Quartus II software. After the license expires, you can obtain another license file from the Altera web site and install it to continue compiling time-limited versions.

Getting Started

After you have installed the MegaCore functions, and obtained and set up your OpenCore Plus license, you are ready to begin your design. The following steps describe the design process using a time-limited version of the core.

1. Run the Quartus II or MAX+PLUS II software.
2. Add user libraries pointing to the OpenCore Plus hardware evaluation version of each MegaCore function you want to use. The libraries are located in `<installation path>\<MegaCore function>\lib_time_limited`.



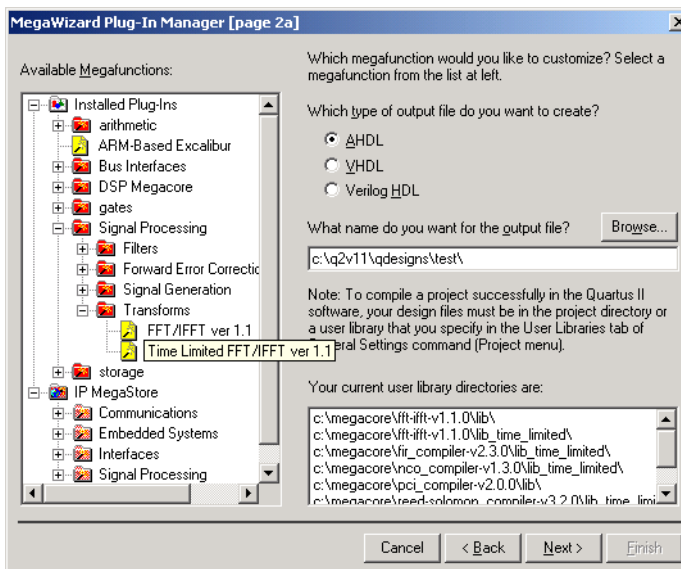
Refer to Quartus II or MAX+PLUS II Help for information on how to set up user libraries.

3. Start the MegaWizard Plug-in Manager by choosing the **MegaWizard Plug-In Manager** command (File menu in the MAX+PLUS II software and Tools menu in the Quartus II software), or by starting the stand-alone version of the MegaWizard Plug-In Manager by typing the command `megawiz` ↵ at a command prompt. The **MegaWizard Plug-In Manager** dialog box displays.

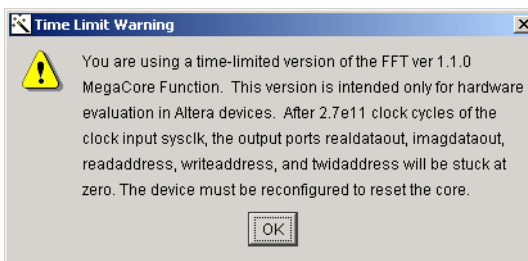


Refer to Quartus II or MAX+PLUS II Help for instructions on how to use the MegaWizard Plug-In Manager.

4. Choose the time-limited version of the core. See [Figure 2 on page 5](#).

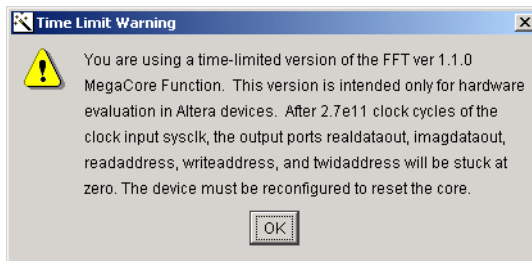
Figure 2. Choose the Time-Limited Version in the MegaWizard Plug-In Manager

When you choose a time-limited core, you will receive a warning message similar to the one shown in [Figure 3](#).

Figure 3. OpenCore Plus Warning Message

- Continue through the rest of the wizard as described in the user guide for the MegaCore function.

When you have finished setting parameters using the wizard, you will receive time limit warning message similar to the one shown in [Figure 4](#) on page 6.

Figure 4. Time Limit Warning Message

The time limit warning message specifies how many clocks the core will run before it expires, as well as the behavior of the core after it is disabled.

6. Implement the wizard-generated output files in your design.

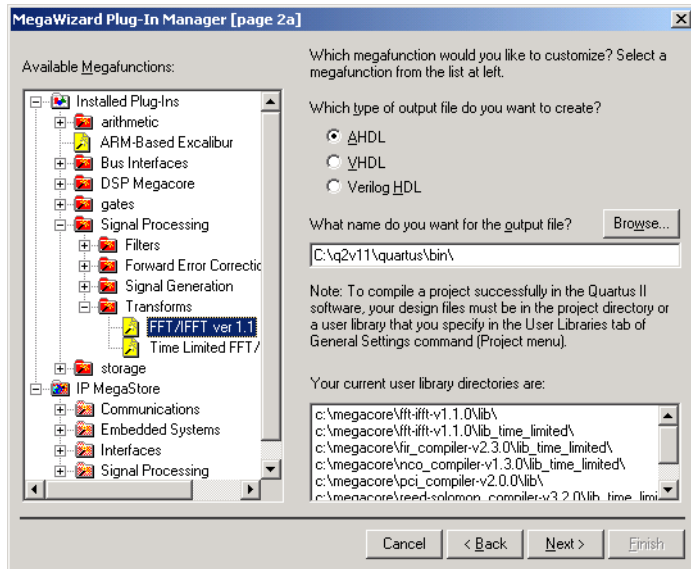


If you want to perform time-limited hardware evaluation (and you have not purchased licenses for any MegaCore functions), you can only use MegaCore functions that support the OpenCore Plus feature in your design. Otherwise, the Quartus II or MAX+PLUS II software will not generate programming files. For example, if you use a time-limited NCO compiler function in the same design with a non-time-limited FIR compiler function, no programming files will be generated.

After you have finished hardware testing your design using the OpenCore Plus feature, you are ready to purchase a license for the MegaCore function(s). Perform the following steps to complete your design.

1. Purchase a license for the MegaCore function you want to use.
2. Install your MegaCore license.
3. Run the Quartus II or MAX+PLUS II software.
4. Add user libraries pointing to the standard MegaCore library (if you have not already done so). The libraries are located in *<installation path>\<MegaCore function>\lib*.
5. Choose the standard (non-time-limited) version of the core. See [Figure 5 on page 7](#). Go through the standard (non-time-limited) MegaCore wizard, setting the parameters for your design.

Figure 5. Choose the Standard Version in the MegaWizard Plug-In Manager



You must re-enter all parameters in the wizard for the standard MegaCore function, even if you have already entered the same parameters for the time-limited version.

6. Drop the non-time-limited wizard output files into your design, replacing the time-limited ones.
7. Compile your design and program or configure the Altera devices.



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